Vignesh vlsi

List of Publications by Year
in descending order

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Version: 2024-02-01

27	117	1937457	1588896
papers	citations	4	8
		h-index	g-index

31	31	31	64
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Daily evapotranspiration prediction using gradient boost regression model for irrigation planning. Journal of Supercomputing, 2020, 76, 5732-5744.	2.4	32
2	An Embedded systems approach to monitor green house. , 2010, , .		28
3	Performance Analysis of Real Time Operating System with General Purpose Operating System for Mobile Robotic System. Indian Journal of Science and Technology, 2015, 8, .	0.5	13
4	Analysis and Implementation of High Performance Reconfigurable Finite Impulse Response Filter Using Distributed Arithmetic. Wireless Personal Communications, 2018, 102, 3413-3425.	1.8	9
5	DA-Based Efficient Testable FIR Filter Implementation on FPGA Using Reversible Logic. Circuits, Systems, and Signal Processing, 2014, 33, 863-884.	1.2	4
6	A paradigm of distributed arithmetic (DA) approaches for digital FIR filter. , 2016, , .		4
7	An Efficient Low Power and High Speed Distributed Arithmetic Design for FIR Filter. Indian Journal of Science and Technology, 2016, 9, .	0.5	4
8	A novel method to compress voice signal using compressive sensing. , 2015, , .		3
9	Reliability improved, high performance FIR filter design using new computation sharing multiplier: suitable for signal processing applications. Cluster Computing, 2019, 22, 13669-13681.	3.5	2
10	Low-power and high-throughput 128-point feedforward FFT processor. Cluster Computing, 2019, 22, 13397-13404.	3.5	2
11	A Novel Less Area Computation Sharing High Speed Multiplier Architecture for FIR Filter Design. Research Journal of Applied Sciences, Engineering and Technology, 2015, 10, 816-823.	0.1	1
12	A Novel Approach to Compress an Image Using Cascaded Transform and Compressive Sensing. Advances in Intelligent Systems and Computing, 2016, , 743-749.	0.5	1
13	Design of Arithmetic and Logic Unit (ALU) Using Subthreshold Adiabatic Logic for Low-Power Application. Lecture Notes in Electrical Engineering, 2018, , 201-209.	0.3	1
14	Characterization and modeling of dual material double gate tunnel field effect transistor using superposition approximation method. Concurrency Computation Practice and Experience, 2019, 31, e4860.	1.4	1
15	Reconfigurable communication wrapper for QoS demand for network on chip. International Journal of Advanced Intelligence Paradigms, 2019, 12, 24.	0.2	1
16	Design of digital FIR filter using dynamic distributed arithmetic algorithm with improved table look up scheme for residue number system. , 2007, , .		1
17	A Novel Cascaded Image Transform by Varying Energy Density to Convert an Image in to Sparse. Indian Journal of Science and Technology, 2015, 8, 766.	0.5	1
18	VLSI Architectures for Lifting Based Discrete Wavelet Transform â€“ A Survey. Indonesian Journal of Electrical Engineering and Computer Science, 2016, 3, 323.	0.7	1

#	ARTICLE	IF	CITATIONS
19	Linear transformation based efficient canonical signed digit multiplier using high speed and low power reversible logic. , 2012, , .		0
20	Fuzzy controller for error control of on â€" Chip communication. , 2017, , .		0
21	Genetic algorithm based on-chip communication link reconfiguration for efficient on-chip communication. , 2017, , .		0
22	High Performance Trench Gate Power MOSFET of Indium Phosphide. Lecture Notes in Electrical Engineering, 2018, , 175-181.	0.3	0
23	An adaptive low power coding scheme for the NoC. International Journal of Advanced Intelligence Paradigms, 2019, 13, 324.	0.2	0
24	Design of high performance filter bank multi-carrier transmitter. Cluster Computing, 2019, 22, 12521-12527.	3.5	0
25	Analog to information convertor using cascaded transform and Gaussian random matrix. Cluster Computing, 2019, 22, 11813-11820.	3.5	0
26	DESIGN OF HIGH PERFORMANCE MULTIPLIERLESS LINEAR PHASE FINITE IMPULSE RESPONSE FILTERS. Asian Journal of Pharmaceutical and Clinical Research, 2017, 10, 66.	0.3	0
27	OPTIMIZING TWIDDLE FACTOR MULTIPLICATION UNITS OF 128-POINT FAST FOURIER TRANSFORM FOR 5G IMPLEMENTATION. Far East Journal of Electronics and Communications, 2017, 17, 845-861.	0.2	0