Nuno M C Paulino

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/261493/publications.pdf

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17	73	1684188 5	1720034 7
papers	citations	h-index	g-index

17	17	17	32
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Transparent Trace-Based Binary Acceleration for Reconfigurable HW/SW Systems. IEEE Transactions on Industrial Informatics, 2013, 9, 1625-1634.	11.3	12
2	Improving Performance and Energy Consumption in Embedded Systems via Binary Acceleration: A Survey. ACM Computing Surveys, 2021, 53, 1-36.	23.0	9
3	From Instruction Traces to Specialized Reconfigurable Arrays. , 2011, , .		8
4	Transparent Runtime Migration of Loop-Based Traces of Processor Instructions to Reconfigurable Processing Units. International Journal of Reconfigurable Computing, 2013, 2013, 1-20.	0.2	7
5	Dynamic Partial Reconfiguration of Customized Single-Row Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 116-125.	3.1	7
6	Transparent Acceleration of Program Execution using Reconfigurable Hardware. , 2015, , .		6
7	Generation of Customized Accelerators for Loop Pipelining of Binary Instruction Traces. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 21-34.	3.1	6
8	Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support. , 2014, , .		4
9	Evaluating a Novel Bluetooth 5.1 AoA Approach for Low-Cost Indoor Vehicle Tracking via Simulation. , 2021, , .		4
10	A Reconfigurable Architecture for Binary Acceleration of Loops with Memory Accesses. ACM Transactions on Reconfigurable Technology and Systems, 2015, 7, 1-20.	2.5	3
11	Optimizing OpenCL Code for Performance on FPGA: k-Means Case Study With Integer Data Sets. IEEE Access, 2020, 8, 152286-152304.	4.2	2
12	A Binary Translation Framework for Automated Hardware Generation. IEEE Micro, 2021, 41, 15-23.	1.8	2
13	Architecture for Transparent Binary Acceleration of Loops with Memory Accesses. Lecture Notes in Computer Science, 2013, , 122-133.	1.3	2
14	Optimizing Packet Reception Rates for Low Duty-Cycle BLE Relay Nodes. IEEE Sensors Journal, 2022, 22, 13753-13762.	4.7	1
15	Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework. , 2020, , .		0
16	On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators. , 2021, , .		0
17	FPGAs as General-Purpose Accelerators for Non-Experts via HLS: The Graph Analysis Example. , 2021, , .		0