Jesus R Urresti

List of Publications by Year
in descending order

23	227	1478505 6	1125743 13
papers	citations	h-index	g-index

23	23	23	207
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	UIS failure mechanism of SiC power MOSFETs. , 2016, , .		36
2	Analysis of hot-carrier degradation in a SOI LDMOS transistor with a steep retrograde drift doping profile. Microelectronics Reliability, 2005, 45, 493-498.	1.7	31
3	A Comprehensive Study on the Avalanche Breakdown Robustness of Silicon Carbide Power MOSFETs. Energies, 2017, 10, 452.	3.1	31
4	Increased Mobility in Enhancement Mode 4H-SiC MOSFET Using a Thin SiO₂/ Al₂O₃Gate Stack. IEEE Electron Device Letters, 2018, 39, 564-567.	3.9	27
5	A numerical study of field plate configurations in RF SOI LDMOS transistors. Solid-State Electronics, 2006, 50, 155-163.	1.4	21
6	Influence of gate bias on the avalanche ruggedness of SiC power MOSFETs. , 2017, , .		15
7	Design and Analysis of High Mobility Enhancement-Mode 4H-SiC MOSFETs Using a Thin-SiO2/Al2O3 Gate-Stack. IEEE Transactions on Electron Devices, 2019, 66, 1710-1716.	3.0	15
8	Modeling of non-uniform heat generation in LDMOS transistors. Solid-State Electronics, 2005, 49, 77-84.	1.4	9
9	Efficiency of SOI-Like Structures for Reducing the Thermal Resistance in Thin-Film SOI Power LDMOSFETs. IEEE Electron Device Letters, 2004, 25, 743-745.	3.9	7
10	Lateral punch-through TVS devices for on-chip protection in low-voltage applications. Microelectronics Reliability, 2005, 45, 1181-1186.	1.7	6
11	Optimisation of very low voltage TVS protection devices. Microelectronics Journal, 2003, 34, 809-813.	2.0	5
12	Analysis and optimization of safe-operating-area of LUDMOS transistors based on 0.18 Âµm SOI CMOS technology. Semiconductor Science and Technology, 2010, 25, 045013.	2.0	5
13	Study of layout influence on ruggedness of NPT-IGBT devices by physical modelling. Microelectronics Reliability, 2012, 52, 2471-2476.	1.7	4
14	IGBT design optimisation for solid-state circuit breaker applications. , 2013, , .		4
15	Degradation analysis in SOI LDMOS transistors with steep retrograde doping profile and source field plate. , 0, , .		3
16	A quasi-analytical breakdown voltage model in four-layer punch-through TVS devices. Solid-State Electronics, 2005, 49, 1309-1313.	1.4	2
17	Lateral Punch-Through TVS Devices: Design and Fabrication. , 2009, , .		2
18	High Mobility 4H-SiC MOSFET. , 2018, , .		2

#	Article	IF	Citations
19	Non-uniform temperature and heat generation in thin-film SOI LDMOS with uniform drift doping. IET Circuits, Devices and Systems, 2006, 153, 82.	0.6	1
20	3.3 kV PTâ€IGBT with voltageâ€sensor monolithically integrated. IET Circuits, Devices and Systems, 2014, 8, 182-187.	1.4	1
21	A physically based thermal model for high-voltage thin-film SOI LDMOS in short circuit operation. Physica Status Solidi (A) Applications and Materials Science, 2005, 202, 1862-1868.	1.8	0
22	Volatge-sensor monolithically integrated in 3.3 kV IGBTs. , 2011, , .		0
23	Overload robust IGBT design for SSCB application. Microelectronics Reliability, 2014, 54, 1906-1910.	1.7	0