Kimihiko Kato

List of Publications by Year
in descending order

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70	504	758635 12	839053 18
papers	citations	h-index	g-index

70	70	70	573
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Programming Nanoparticles in Multiscale: Optically Modulated Assembly and Phase Switching of Silicon Nanoparticle Array. ACS Nano, 2018, 12, 2231-2241.	7.3	32
2	Effects of ZrO₂/Al₂O₃ Gate-Stack on the Performance of Planar-Type InGaAs TFET. IEEE Transactions on Electron Devices, 2019, 66, 1862-1867.	1.6	25
3	Experimental observation of type-I energy band alignment in lattice-matched Ge1â^'xâ^'ySixSny/Ge heterostructures. Applied Physics Letters, 2016, 108, .	1.5	23
4	Stabilized formation of tetragonal ZrO2 thin film with high permittivity. Thin Solid Films, 2014, 557, 192-196.	0.8	22
5	Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching. IEEE Electron Device Letters, 2016, 37, 31-34.	2.2	20
6	Formation processes of Ge3N4 films by radical nitridation and their electrical properties. Thin Solid Films, 2010, 518, S226-S230.	0.8	19
7	Formation of high-quality oxide/Ge1â^'xSnx interface with high surface Sn content by controlling Sn migration. Applied Physics Letters, 2014, 105, 122103.	1.5	19
8	Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic. IEEE Electron Device Letters, 2016, 37, 1563-1565.	2.2	17
9	Improvement of Al2O3/Ge interfacial properties by O2-annealing. Thin Solid Films, 2012, 520, 3397-3401.	0.8	16
10	Impacts of AlGeO formation by post thermal oxidation of Al2O3/Ge structure on interfacial properties. Thin Solid Films, 2014, 557, 282-287.	0.8	15
11	p-Channel TFET Operation of Bilayer Structures With Type-II Heterotunneling Junction of Oxide- and Group-IV Semiconductors. IEEE Transactions on Electron Devices, 2020, 67, 1880-1886.	1.6	15
12	Bilayer tunneling field effect transistor with oxide-semiconductor and group-IV semiconductor hetero junction: Simulation analysis of electrical characteristics. AIP Advances, 2019, 9, 055001.	0.6	14
13	A Novel Gate-Normal Tunneling Field-Effect Transistor With Dual-Metal Gate. IEEE Journal of the Electron Devices Society, 2018, 6, 1070-1076.	1.2	13
14	Understanding of interface structures and reaction mechanisms induced by Ge or GeO diffusion in Al2O3/Ge structure. Applied Physics Letters, 2013, 103, .	1.5	12
15	Reduction of Schottky barrier height for n-type Ge contact by using Sn electrode. Japanese Journal of Applied Physics, 2014, 53, 04EA06.	0.8	12
16	Influence of impurity concentration in Ge sources on electrical properties of Ge/Si hetero-junction tunneling field-effect transistors. Applied Physics Letters, 2018, 113, 062103.	1.5	12
17	ZnO/Si and ZnO/Ge bilayer tunneling field effect transistors: Experimental characterization of electrical properties. Journal of Applied Physics, 2019, 125, .	1.1	12
18	TiN/Al2O3/ZnO gate stack engineering for top-gate thin film transistors by combination of post oxidation and annealing. Applied Physics Letters, 2018, 112, .	1.5	11

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19	Electrical characteristic of atomic layer deposition La₂O₃/Si MOSFETs with ferroelectric-type hysteresis. Japanese Journal of Applied Physics, 2019, 58, SBBA05.	0.8	11
20	Robustness of Sn precipitation during thermal oxidation of Ge_{1â^'}_xSn_xon Ge(001). Japanese Journal of Applied Physics, 2014, 53, 08LD04.	0.8	10
21	Metalâ€“oxideâ€“semiconductor interface properties of TiN/Y2O3/Si0.62Ge0.38 gate stacks with high temperature post-metallization annealing. Journal of Applied Physics, 2020, 127, .	1.1	10
22	Interfacial Reaction Mechanisms in Al₂O₃/Ge Structure by Oxygen Radical Process. Japanese Journal of Applied Physics, 2013, 52, 04CA08.	0.8	9
23	Interface properties of Al₂O₃/Ge structures with thin Ge oxide interfacial layer formed by pulsed metal organic chemical vapor deposition. Japanese Journal of Applied Physics, 2014, 53, 08LD03.	0.8	9
24	There's plenty of room at the top. , 2017, , .		9
25	Fabrication of thin body InAs-on-insulator structures by Smart Cut method with H⁺ implantation at room temperature. Japanese Journal of Applied Physics, 2019, 58, SBBA03.	0.8	9
26	Tilted ion implantation as a cost-efficient sublithographic patterning technique. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2016, 34, 040608.	0.6	8
27	RF reflectometry for readout of charge transition in a physically defined p-channel MOS silicon quantum dot. Japanese Journal of Applied Physics, 2021, 60, SBBI07.	0.8	8
28	Fabrication and Electrical Characteristics of ZnSnO/Si Bilayer Tunneling Filed-Effect Transistors. IEEE Journal of the Electron Devices Society, 2019, 7, 1201-1208.	1.2	7
29	Electron beam lithography with negative tone resist for highly integrated silicon quantum bits. Nanotechnology, 2021, 32, 485301.	1.3	7
30	Source engineering for bilayer tunnel field-effect transistor with hetero tunnel junction: thickness and impurity concentration. Applied Physics Express, 2020, 13, 074004.	1.1	7
31	Control of Interfacial Properties of Al₂O₃/Ge Gate Stack Structure Using Radical Nitridation Technique. Japanese Journal of Applied Physics, 2011, 50, 10PE02.	0.8	6
32	Oxygen and germanium migration at low temperature influenced by the thermodynamic nature of the materials used in germanium metal-insulator-semiconductor structures. Applied Physics Letters, 2015, 107, .	1.5	6
33	Sub-lithographic Patterning via Tilted Ion Implantation for Scaling Beyond the 7-nm Technology Node. IEEE Transactions on Electron Devices, 2017, 64, 231-236.	1.6	6
34	Control of interfacial properties of Pr-oxide/Ge gate stack structure by introduction of nitrogen. Solid-State Electronics, 2011, 60, 70-74.	0.8	5
35	Formation of chemically stable GeO2 on the Ge surface with pulsed metalâ€“organic chemical vapor deposition. Applied Physics Letters, 2015, 106, 062107.	1.5	5
36	Thermal properties of IIIâ€“V on a SiC platform for photonic integrated circuits. Japanese Journal of Applied Physics, 2019, 58, SBBE06.	0.8	5

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37	Accurate evaluation of specific contact resistivity between InAs/Niâ€“InAs alloy using a multi-sidewall transmission line method. Japanese Journal of Applied Physics, 2020, 59, SGGA08.	0.8	5
38	Formation and crystalline structure of Ni silicides on Si(110) substrate. Japanese Journal of Applied Physics, 2014, 53, 05GA12.	0.8	4
39	Importance of control of oxidant partial pressure on structural and electrical properties of Pr-oxide films. Thin Solid Films, 2014, 557, 276-281.	0.8	4
40	Enhanced patterning by tilted ion implantation. Proceedings of SPIE, 2016, , .	0.8	4
41	(Invited)Ultra-Low Power III-V-Based MOSFETs and Tunneling FETs. ECS Transactions, 2018, 85, 27-37.	0.3	4
42	Improvement in Electrical Characteristics of ZnSnO/Si Bilayer TFET by W/Alâ„Oâ‚ƒ Gate Stack. IEEE Journal of the Electron Devices Society, 2020, 8, 341-345.	1.2	4
43	Analysis of Local Leakage Current of Pr-Oxide Thin Films with Conductive Atomic Force Microscopy. Japanese Journal of Applied Physics, 2011, 50, 04DA08.	0.8	3
44	Effect of Interfacial Reactions in Radical Process on Electrical Properties of Al2O3/Ge Gate Stack Structure. Journal of Physics: Conference Series, 2013, 417, 012001.	0.3	3
45	(Invited) Ultrathin-Body Ge-on-Insulator MOSFET and TFET Technologies. ECS Transactions, 2018, 86, 75-86.	0.3	3
46	Effect of Pr Valence State on Interfacial Structure and Electrical Properties of Pr Oxide/PrON/Ge Gate Stack Structure. Japanese Journal of Applied Physics, 2011, 50, 04DA17.	0.8	2
47	Effect of gate metal on chemical bonding state in metal/Pr-oxide/Ge gate stack structure. Solid-State Electronics, 2013, 83, 56-60.	0.8	2
48	There's still plenty of room at the bottom â€" And at the Top. , 2017, , .		2
49	ON current enhancement and variability suppression in tunnel FETs by the isoelectronic trap impurity of beryllium. Japanese Journal of Applied Physics, 2021, 60, SBBA01.	0.8	2
50	Advanced CMOS technologies for ultra-low power logic and AI applications. , 2021, , .		2
51	Si bilayer tunnel field-effect transistor structure realized using tilted ion-implantation technique. Solid-State Electronics, 2021, 180, 107993.	0.8	2
52	Effect of Pr Valence State on Interfacial Structure and Electrical Properties of Pr Oxide/PrON/Ge Gate Stack Structure. Japanese Journal of Applied Physics, 2011, 50, 04DA17.	0.8	2
53	Characterization of Damage of Al$_{2}$O$_{3}$/Ge Gate Stack Structure Induced with Light Radiation during Plasma Nitridation. Japanese Journal of Applied Physics, 2012, 51, 01AJ01.	0.8	1
54	Importance of Ge surface oxidation with high oxidation rate in obtaining low interface state density at oxide/Ge interfaces. Japanese Journal of Applied Physics, 2014, 53, 08LD02.	0.8	1

#	Article	IF	Citations
55	Sub-5 nm gap formation for low power NEM switches. , 2015, , .		1
56	Cost-efficient sub-lithographic patterning with tilted-ion implantation (TII). , 2018, , .		1
57	Group IV Based Bi-Layer Tunneling Field Effect Transistor. ECS Transactions, 2019, 93, 23-27.	0.3	1
58	Material design of oxide-semiconductor/group-IV-semiconductor bilayer tunneling field effect transistors. , 2019, , .		1
59	Impact of Switching Voltage on Complementary Steep-Slope Tunnel Field Effect Transistor Circuits. IEEE Transactions on Electron Devices, 2020, 67, 3876-3882.	1.6	1
60	Development of Integrated Device Simulator for Quantum Bit Design: Self-consistent Calculation for Quantum Transport and Qubit Operation. , 2021, , .		1
61	Buried nanomagnet realizing high-speed/low-variability silicon spin qubits: implementable in error-correctable large-scale quantum computers. , 2021, , .		1
62	Mechanism of extraordinary gate-length dependence of quantum dot operation in isoelectronic-trap-assisted tunnel FETs. Applied Physics Express, 2020, 13, 114001.	1.1	1
63	Effects of Light Exposure during Plasma Processing on Electrical Properties of GeO2/Ge Structures. Japanese Journal of Applied Physics, 2013, 52, 01AC04.	0.8	0
64	Sustaining the silicon revolution: From 3-D transistors to 3-D integration. , 2015, , .		0
65	Advanced MOS Device Technology for Low Power Logic LSI. , 2019, , .		0
66	(Invited) Tunneling FET Device Technology for Ultra-Low Power Integrated Circuits. ECS Transactions, 2019, 92, 59-69.	0.3	0
67	Fabrication of High Quality InAs-on-Lnsulator Structures by Smart Cut Process with Reuse of InAs Wafers. , 2019, , .		0
68	7â€5: Invited Paper: Bilayer Tunneling Field Effect Transistors using Oxide Semiconductor/Groupâ€IV Semiconductor Heteroâ€structures. Digest of Technical Papers SID International Symposium, 2021, 52, 73-76.	0.1	0
69	4.2ÂK sensitivity-tunable radio frequency reflectometry of a physically defined p-channel silicon quantum dot. Scientific Reports, 2021, 11, 20039.	1.6	0
70	Group IV/oxide semiconductor bi-layer tunneling FET. , 2019, , .		0