Anubha Goel

List of Publications by Year
in descending order

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12	257	1307594	1474206
papers	citations	7 h-index	9 g-index

12	12	12	71
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Dielectric Modulated Junctionless Biotube FET (DM-JL-BT-FET) Bio-Sensor. IEEE Sensors Journal, 2021, 21, 16731-16743.	4.7	43
2	Temperature-Dependent Gate-Induced Drain Leakages Assessment of Dual-Metal Nanowire Field-Effect Transistorâ€"Analytical Model. IEEE Transactions on Electron Devices, 2019, 66, 2437-2445.	3.0	41
3	High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for high frequency applications. Microsystem Technologies, 2020, 26, 1697-1705.	2.0	36
4	Shallow Extension Engineered Dual Material Surrounding Gate (SEE-DM-SG) MOSFET for improved gate leakages, analysis of circuit and noise performance. AEU - International Journal of Electronics and Communications, 2019, 111, 152924.	2.9	28
5	Novel Dual-Metal Junctionless Nanotube Field-Effect Transistors for Improved Analog and Low-Noise Applications. Journal of Electronic Materials, 2021, 50, 108-119.	2.2	28
6	Physics-based analytic modeling and simulation of gate-induced drain leakage and linearity assessment in dual-metal junctionless accumulation nano-tube FET (DM-JAM-TFET). Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	26
7	Modeling of shallow extension engineered dual metal surrounding gate (SEE-DM-SG) MOSFET gate-induced drain leakage (GIDL). Indian Journal of Physics, 2021, 95, 299-308.	1.8	25
8	Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA)for DNA Bio-Molecule Detection. , 2018, , .		13
9	Enhanced Analog Performance and High-Frequency Applications of Dielectric Engineered High-K Schottky Nanowire FET. Silicon, 2022, 14, 9733-9749.	3.3	7
10	GaN based Dual-Metal Gate Stack Engineered Junctionless-Surrounding-Gate (DMSEJSG) MOSFET for High Power Applications. , 2019, , .		4
11	<scp>SiC</scp>â€based analytical model for gateâ€stack dual metal nanowire<scp>FET</scp>with enhanced analog performance. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2022, 35, .	1.9	4
12	Linearity and Intermodulation Distortion Assessment of Underlap Engineered Cylindrical Junctionless Surrounding Gate MOSFET for Low Noise CMOS RFIC Design. , 2019, , .		2