Masanori Hashimoto

List of Publications by Year in Descending Order

173 papers	871 citations	14 h-index	20 g-index
237 ext. papers	1,141 ext. citations	1.3 avg, IF	4.42 L-index

#	Paper	IF	Citations
173	VirtualSync+: Timing Optimization with Virtual Synchronization. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
172	Impact of Neutron-Induced SEU in FPGA CRAM on Image-Based Lane Tracking for Autonomous Driving: From Bit Upset to SEFI and Erroneous Behavior. *IEEE Transactions on Nuclear Science*, **2021**, 1-1	1.7	
171	Via-Switch FPGA: 65-nm CMOS Implementation and Evaluation. *IEEE Journal of Solid-State Circuits*, **2021**, 1-1	5.5	1
170	. *IEEE Transactions on Nuclear Science*, **2021**, 68, 1228-1234	1.7	
169	Make it Trackable: An Instant Magnetic Tracking System With Coil-Free Tiny Trackers. *IEEE Access*, **2021**, 9, 26616-26632	3.5	2
168	MUX Granularity Oriented Iterative Technology Mapping for Implementing Compute-Intensive Applications on Via-Switch FPGA **2021**,		1
167	Analyzing DUE Errors on GPUs With Neutron Irradiation Test and Fault Injection to Control Flow. *IEEE Transactions on Nuclear Science*, **2021**, 68, 1668-1674	1.7	3
166	When Single Event Upset Meets Deep Neural Networks: Observations, Explorations, and Remedies **2020**,		9
165	Logarithm-approximate floating-point multiplier is applicable to power-efficient neural network training. *The Integration VLSI Journal*, **2020**, 74, 19-31	1.4	3
164	Angular Sensitivity of Neutron-Induced Single-Event Upsets in 12-nm FinFET SRAMs With Comparison to 20-nm Planar SRAMs. *IEEE Transactions on Nuclear Science*, **2020**, 67, 1485-1493	1.7	3
163	Measurement of Single-Event Upsets in 65-nm SRAMs Under Irradiation of Spallation Neutrons at J-PARC MLF. *IEEE Transactions on Nuclear Science*, **2020**, 1-1	1.7	2
162	Impact of the Angle of Incidence on Negative Muon-Induced SEU Cross Sections of 65-nm Bulk and FDSOI SRAMs. *IEEE Transactions on Nuclear Science*, **2020**, 67, 1566-1572	1.7	
161	33.3 Via-Switch FPGA: 65nm CMOS Implementation and Architecture Extension for Al Applications **2020**,		2
160	Irradiation Test of 65-nm Bulk SRAMs With DC Muon Beam at RCNP-MuSIC Facility. *IEEE Transactions on Nuclear Science*, **2020**, 67, 1555-1559	1.7	2
159	Soft Error and Its Countermeasures in Terrestrial Environment **2020**,		3
158	Fault Diagnosis of Via-Switch Crossbar in Non-volatile FPGA **2020**,		2
157	Feasibility Evaluation on an Instant Invader Detection System with Ultrasonic Sensors Scattered on the Ground. *International Journal on Smart Sensing and Intelligent Systems*, **2020**, 7, 1-6	0.4	

156	A Fault Detection and Diagnosis Method for Via-Switch Crossbar in Non-Volatile FPGA. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2020**, E103.A, 1447-1455	0.4	1
155	DC Magnetic Field Based 3D Localization With Single Anchor Coil. *IEEE Sensors Journal*, **2020**, 20, 3902-3913	4	5
154	Sneak Path Free Reconfiguration With Minimized Programming Steps for Via-Switch Crossbar-Based FPGA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 2572-2587	2.5	2
153	Position and Posture Estimation of Capsule Endoscopy with a Single Wearable Coil Toward Daily Life Diagnosis **2020**,		1
152	BYNQNet: Bayesian Neural Network with Quadratic Activations for Sampling-Free Uncertainty Estimation on FPGA **2020**,		4
151	Impact of Hydrided and Non-Hydrided Materials Near Transistors on Neutron-Induced Single Event Upsets **2020**,		2
150	A Frequency-Dependent Target Impedance Method Fulfilling Voltage Drop Constraints in Multiple Frequency Ranges. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2020**, 10, 1769-1781	1.7	2
149	Characterizing Energetic Dependence of Low-Energy Neutron-induced MCUs in 65 nm bulk SRAMs **2020**,		2
148	A Multicore Chip Load Model for PDN Analysis Considering Voltage□Current-Timing Interdependency and Operation Mode Transitions. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2019**, 9, 1669-1679	1.7	1
147	A Frequency-Dependent Target Impedance Method Fulfilling Both Average and Dynamic Voltage Drop Constraints **2019**,		1
146	Editorial TVLSI Positioning□Continuing and Accelerating an Upward Trajectory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 253-280	2.6	4
145	Analyzing Impacts of SRAM, FF and Combinational Circuit on Chip-Level Neutron-Induced Soft Error Rate. *IEICE Transactions on Electronics*, **2019**, E102.C, 296-302	0.4	4
144	Impact of Irradiation Side on Neutron-Induced Single-Event Upsets in 65-nm Bulk SRAMs. *IEEE Transactions on Nuclear Science*, **2019**, 66, 1374-1380	1.7	6
143	Characterizing SRAM and FF soft error rates with measurement and simulation. *The Integration VLSI Journal*, **2019**, 69, 161-179	1.4	6
142	Similarity Analysis on Neutron- and Negative Muon-Induced MCUs in 65-nm Bulk SRAM. *IEEE Transactions on Nuclear Science*, **2019**, 66, 1390-1397	1.7	9
141	Estimation of Muon-Induced SEU Rates for 65-nm Bulk and UTBB-SOI SRAMs. *IEEE Transactions on Nuclear Science*, **2019**, 66, 1398-1403	1.7	6
140	. *IEEE Transactions on Electron Devices*, **2019**, 66, 3331-3336	2.9	6
139	Applications of Reconfigurable Processors as Embedded Automatons in the IoT Sensor Networks in Space **2019**, 735-750		

138	Time-Dependent Degradation in Device Characteristics and Countermeasures by Design **2019**, 203-243		
137	MTTF-Aware Design Methodology of Adaptively Voltage Scaled Circuit with Timing Error Predictive Flip-Flop. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2019**, E102.A, 867-877	0.4	0
136	Stochastic Analysis on Hold Timing Violation in Ultra-Low Temperature Circuits for Functional Test at Room Temperature. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2019**, E102.A, 914-917	0.4	
135	Radiation-Induced Soft Errors **2019**, 57-127		2
134	Distilling Knowledge for Non-Neural Networks **2019**,		2
133	Minimizing Power for Neural Network Training with Logarithm-Approximate Floating-Point Multiplier **2019**,		1
132	Sensor Signal Processing Using High-Level Synthesis With a Layered Architecture. *IEEE Embedded Systems Letters*, **2018**, 10, 119-122	1	1
131	MTTF-aware design methodology of error prediction based adaptively voltage-scaled circuits **2018**,		1
130	Via-Switch FPGA: Highly Dense Mixed-Grained Reconfigurable Architecture With Overlay Via-Switch Crossbars. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2723-2736	2.6	10
129	Near-future traffic evaluation based navigation for automated driving vehicles considering traffic uncertainties **2018**,		1
128	An on-chip load model for off-chip PDN analysis considering interdependency between supply voltage, current profile and clock latency **2018**,		1
127	Activation-Aware Slack Assignment for Time-to-Failure Extension and Power Saving. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 2217-2229	2.6	2
126	From Process Variations to Reliability: A Survey of Timing of Digital Circuits in the Nanometer Era. *IPSJ Transactions on System LSI Design Methodology*, **2018**, 11, 2-15	0.2	4
125	Virtualsync **2018**,		8
124	Sneak path free reconfiguration of via-switch crossbars based FPGA **2018**,		2
123	An analytic evaluation on soft error immunity enhancement due to temporal triplication. *International Journal of Embedded Systems*, **2018**, 10, 22	0.5	0
122	Hardware Architecture for High-Speed Object Detection Using Decision Tree Ensemble. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2018**, E101.A, 1298-1307	0.4	3
121	Measurement and Mechanism Investigation of Negative and Positive Muon-Induced Upsets in 65-nm Bulk SRAMs. *IEEE Transactions on Nuclear Science*, **2018**, 65, 1734-1741	1.7	12

120	Negative and Positive Muon-Induced Single Event Upsets in 65-nm UTBB SOI SRAMs. *IEEE Transactions on Nuclear Science*, **2018**, 65, 1742-1749	1.7	6
119	MTTF-aware design methodology for adaptive voltage scaling **2018**,		1
118	Minimizing detection-to-boosting latency toward low-power error-resilient circuits. *The Integration VLSI Journal*, **2017**, 58, 236-244	1.4	
117	Impedance matching in magnetic-coupling-resonance wireless power transfer for small implantable devices **2017**,		3
116	Contributions of SRAM, FF and combinational circuit to chip-level neutron-induced soft error rate: - Bulk vs. FD-SOI at 0.5 and 1.0V - **2017**,		1
115	Dedicated antenna less power efficient OOK transmitter for mm-cubic IoT nodes **2017**,		1
114	Soft error rate estimation with TCAD and machine learning **2017**,		5
113	Performance Evaluation of Software-Based Error Detection Mechanisms for Supply Noise Induced Timing Errors. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2017**, E100.A, 1452-1463	0.4	
112	Novel processor architecture for onboard infrared sensors **2016**,		1
111	Multiple sensitive volume based soft error rate estimation with machine learning **2016**,		12
110	Critical path isolation for time-to-failure extension and lower voltage operation **2016**,		4
109	Characterizing Alpha- and Neutron-Induced SEU and MCU on SOTB and Bulk 0.4-V SRAMs. *IEEE Transactions on Nuclear Science*, **2015**, 62, 420-427	1.7	18
108	An oscillator-based true random number generator with process and temperature tolerance **2015**,		5
107	Soft error immune latch design for 20 nm bulk CMOS **2015**,		1
106	Proximity distance estimation based on electric field communication between 1 mm3 sensor nodes. *Analog Integrated Circuits and Signal Processing*, **2015**, 85, 425-432	1.2	0
105	Impact of package on neutron induced single event upset in 20 nm SRAM **2015**,		1
104	**2015**,		2
103	Real-time on-chip supply voltage sensor and its application to trace-based timing error localization **2015**,		5

102	Stochastic timing error rate estimation under process and temporal variations **2015**,		4
101	Modeling the Effect of Global Layout Pattern on Wire Width Variation for On-the-Fly Etching Process Modification. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2015**, E98.A, 1467-1474	0.4	
100	Device-Parameter Estimation with Sensitivity-Configurable Ring Oscillator. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2015**, E98.A, 2607-2613	0.4	
99	Measurement and Analysis of Alpha-Particle-Induced Soft Errors and Multiple-Cell Upsets in 10T Subthreshold SRAM. *IEEE Transactions on Device and Materials Reliability*, **2014**, 14, 463-470	1.6	14
98	Exploring Well-Configurations for Minimizing Single Event Latchup. *IEEE Transactions on Nuclear Science*, **2014**, 61, 3282-3289	1.7	7
97	A Process and Temperature Tolerant Oscillator-Based True Random Number Generator. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 2393-2399	0.4	10
96	Reliability-Configurable Mixed-Grained Reconfigurable Array Supporting C-Based Design and Its Irradiation Testing. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 2518-2529	0.4	8
95	SET Pulse-Width Measurement Suppressing Pulse-Width Modulation and Within-Die Process Variation Effects. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 1461-1467	0.4	
94	NBTI Mitigation Method by Inputting Random Scan-In Vectors in Standby Time. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 1483-1491	0.4	0
93	Edge-over-Erosion Error Prediction Method Based on Multi-Level Machine Learning Algorithm. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 2373-2382	0.4	2
92	Comparative Evaluation of Lifetime Enhancement with Fault Avoidance on Dynamically Reconfigurable Devices. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2014**, E97.A, 1468-1482	0.4	2
91	Mitigating Multi-Bit-Upset With Well-Slits in 28 nm Multi-Bit-Latch. *IEEE Transactions on Nuclear Science*, **2013**, 60, 4362-4367	1.7	3
90	Soft-Error in SRAM at Ultra-Low Voltage and Impact of Secondary Proton in Terrestrial Environment. *IEEE Transactions on Nuclear Science*, **2013**, 60, 4232-4237	1.7	12
89	Impact of NBTI-Induced Pulse-Width Modulation on SET Pulse-Width Measurement. *IEEE Transactions on Nuclear Science*, **2013**, 60, 2630-2634	1.7	14
88	Reliability-configurable mixed-grained reconfigurable array supporting C-to-array mapping and its radiation testing **2013**,		6
87	Real-Time Supply Voltage Sensor for Detecting/Debugging Electrical Timing Failures **2013**,		5
86	A Worst-Case-Aware Design Methodology for Noise-Tolerant Oscillator-Based True Random Number Generator With Stochastic Behavior Modeling. *IEEE Transactions on Information Forensics and Security*, **2013**, 8, 1331-1342	8	18
85	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 2165-2178	2.6	16

84	Stochastic error rate estimation for adaptive speed control with field delay testing **2013**,		6
83	**2013**,		4
82	A process and temperature tolerant oscillator-based true random number generator with dynamic 0/1 bias correction **2013**,		13
81	A gate-delay model focusing on current fluctuation over wide range of process□oltage□emperature variations. *The Integration VLSI Journal*, **2013**, 46, 345-358	1.4	6
80	Supply Noise Suppression by Triple-Well Structure. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 781-785	2.6	10
79	A 0.8-V 110-nA CMOS current reference circuit using subthreshold operation. *IEICE Electronics Express*, **2013**, 10, 20130022-20130022	0.5	2
78	PVT-induced timing error detection through replica circuits and time redundancy in reconfigurable devices. *IEICE Electronics Express*, **2013**, 10, 20130081-20130081	0.5	3
77	Ultra Low Voltage Subthreshold Circuit Design. *Ieice Ess Fundamentals Review*, **2013**, 7, 30-37	0.1	
76	Field Slack Assessment for Predictive Fault Avoidance on Coarse-Grained Reconfigurable Devices. *IEICE Transactions on Information and Systems*, **2013**, E96.D, 1624-1631	0.6	
75	Jitter Amplifier for Oscillator-Based True Random Number Generator. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2013**, E96.A, 684-696	0.4	4
74	Signal-Dependent Analog-to-Digital Conversion Based on MINIMAX Sampling. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2013**, E96.A, 459-468	0.4	2
73	SET pulse-width measurement eliminating pulse-width modulation and within-die process variation effects **2012**,		5
72	Angular Dependency of Neutron-Induced Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM. *IEEE Transactions on Nuclear Science*, **2012**, 59, 2791-2795	1.7	12
71	Signal-dependent analog-to-digital converter based on MINIMAX sampling **2012**,		1
70	Adaptive Performance Compensation With In-Situ Timing Error Predictive Sensors for Subthreshold Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 333-343	2.6	36
69	A predictive delay fault avoidance scheme for coarse-grained reconfigurable architecture **2012**,		1
68	Power Gating Implementation for Supply Noise Mitigation with Body-Tied Triple-Well Structure. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95.A, 2220-2225	0.4	
67	Power Distribution Network Optimization for Timing Improvement with Statistical Noise Model and Timing Analysis. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95.A, 2261-2271	0.4	

66	A Body Bias Clustering Method for Low Test-Cost Post-Silicon Tuning. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95.A, 2292-2300	0.4	
65	An oscillator-based true random number generator with jitter amplifier **2011**,		9
64	Neutron induced single event multiple transients with voltage scaling and body biasing **2011**,		34
63	An Average-Performance-Oriented Subthreshold Processor Self-Timed by Memory Read Completion. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2011**, 58, 299-303	3.5	5
62	Device-parameter estimation with on-chip variation sensors considering random variability **2011**,		3
61	**2011**,		1
60	Implications of Reliability Enhancement Achieved by Fault Avoidance on Dynamically Reconfigurable Architectures **2011**,		2
59	Signal-dependent analog-to-digital conversion based on MINIMAX sampling **2011**,		1
58	Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM. *IEEE Transactions on Nuclear Science*, **2011**, 58, 2097-2102	1.7	18
57	Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2011**, E94-A, 1948-1953	0.4	
56	NBTI Mitigation by Giving Random Scan-in Vectors during Standby Mode. *Lecture Notes in Computer Science*, **2011**, 152-161	0.9	
55	Extracting Device-Parameter Variations with RO-Based Sensors. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2011**, E94-A, 2537-2544	0.4	1
54	Stress Probability Computation for Estimating NBTI-Induced Delay Degradation. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2011**, E94-A, 2545-2553	0.4	0
53	A Design Procedure for Oscillator-Based Hardware Random Number Generator with Stochastic Behavior Modeling. *Lecture Notes in Computer Science*, **2011**, 107-121	0.9	1
52	Setup time, hold time and clock-to-Q delay computation under dynamic supply noise **2010**,		4
51	Gate delay estimation in STA under dynamic power supply noise **2010**,		14
50	Comparative study on delay degrading estimation due to NBTI with circuit/instance/transistor-level stress probability consideration **2010**,		9
49	Transistor Variability Modeling and its Validation With Ring-Oscillation Frequencies for Body-Biased Subthreshold Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1118-1129	2.6	6

48	Modeling the Overshooting Effect for CMOS Inverter Delay Analysis in Nanometer Technologies. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 250-260	2.5	27
47	Measurement circuits for acquiring SET pulsewidth distribution with sub-FO1-inverter-delay resolution **2010**,		12
46	Evaluation of power gating structures focusing on power supply noise with measurement and simulation **2010**,		4
45	Alpha-particle-induced soft errors and multiple cell upsets in 65-nm 10T subthreshold SRAM **2010**,		18
44	Accuracy Enhancement of Grid-Based SSTA by Coefficient Interpolation. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 2441-2446	0.4	
43	Impact of Self-Heating in Wire Interconnection on Timing. *IEICE Transactions on Electronics*, **2010**, E93-C, 388-392	0.4	
42	Gate Delay Estimation in STA under Dynamic Power Supply Noise. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 2447-2455	0.4	2
41	Statistical Timing Analysis Considering Clock Jitter and Skew due to Power Supply Noise and Process Variation. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 2399-2408	0.4	2
40	Prediction of Self-Heating in Short Intra-Block Wires. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 583-594	0.4	
39	Measurement Circuits for Acquiring SET Pulse Width Distribution with Sub-FO1-Inverter-Delay Resolution. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 2417-2423	0.4	7
38	A case for exploiting complex arithmetic circuits towards performance yield enhancement **2009**,		1
37	Tuning-friendly body bias clustering for compensating random variability in subthreshold circuits **2009**,		5
36	Interconnect Modeling: A Physical Design Perspective. *IEEE Transactions on Electron Devices*, **2009**, 56, 1840-1851	2.9	11
35	Adaptive performance compensation with in-situ timing error prediction for subthreshold circuits **2009**,		12
34	Coarse-grained dynamically reconfigurable architecture with flexible reliability **2009**,		24
33	High performance on-chip differential signaling using passive compensation for global communication **2009**,		9
32	Statistical Timing Analysis Considering Spatially and Temporally Correlated Dynamic Power Supply Noise. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2009**, 28, 541-553	2.5	19
31	All-Digital Ring-Oscillator-Based Macro for Sensing Dynamic Supply Noise Waveform. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 1745-1755	5.5	29

30	An Experimental Study on Body-Biasing Layout Style Focusing on Area Efficiency and Speed Controllability. *IEICE Transactions on Electronics*, **2009**, E92-C, 281-285	0.4	1
29	Trade-Off Analysis between Timing Error Rate and Power Dissipation for Adaptive Speed Control with Timing Error Prediction. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 3094-3102	0.4	7
28	Improvement in Computational Accuracy of Output Transition Time Variation Considering Threshold Voltage Variations. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 990-997	0.4	
27	An Approach for Reducing Leakage Current Variation due to Manufacturing Variability. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 3016-3023	0.4	
26	Measurement and Analysis of Inductive Coupling Noise in 90 nm Global Interconnects. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 718-728	5.5	5
25	Clock Skew Evaluation Considering Manufacturing Variability in Mesh-Style Clock Distribution **2008**,		2
24	Measurement of supply noise suppression by substrate and deep N-well in 90nm process **2008**,		9
23	Decoupling capacitance allocation for timing with statistical noise model and timing analysis **2008**,		2
22	Dynamic supply noise measurement circuit composed of standard cells suitable for in-site SoC power integrity verification **2008**,		1
21	Statistical timing analysis considering spatially and temporally correlated dynamic power supply noise **2008**,		4
20	Experimental study on body-biasing layout style-- negligible area overhead enables sufficient speed controllability -- **2008**,		2
19	On-chip high performance signaling using passive compensation **2008**,		2
18	VLSI Timing Verification Considering Delay Variation. *Journal of Japan Institute of Electronics Packaging*, **2008**, 11, 182-185	0.1	
17	Analytical Eye-diagram Model for On-chip Distortionless Transmission Lines and Its Application to Design Space Exploration **2007**,		4
16	Dynamic Supply Noise Measurement with All Digital Gated Oscillator for Evaluating Decoupling Capacitance Effect **2007**,		3
15	Future Prediction of Self-Heating in Short Intra-Block Wires **2007**,		3
14	Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop With On-Chip Delay Measurement. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2007**, 54, 868-872		24
13	Si-substrate Modeling toward Substrate-aware Interconnect Resistance and Inductance Extraction in SoC Design **2006**,		1

List of Publications

12	Measurement of Inductive Coupling Effect on Timing in 90nm Global Interconnects **2006**,		3
11	Measurement results of delay degradation due to power supply noise well correlated with full-chip simulation **2006**,		2
10	Quantitative Prediction of On-chip Capacitive and Inductive Crosstalk Noise and Discussion on Wire Cross-Sectional Area Toward Inductive Crosstalk Free Interconnects. *Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors*, **2006**,		2
9	A Gate Delay Model Focusing on Current Fluctuation over Wide-Range of Process and Environmental Variability. *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers*, **2006**,		2
8	Interconnect capacitance extraction for system LCD circuits **2005**,		2
7	Successive pad assignment algorithm to optimize number and location of power supply pad using incremental matrix inversion **2005**,		5
6	On-chip thermal gradient analysis and temperature flattening for SoC design **2005**,		8
5	Effects of on-chip inductance on power distribution grid **2005**,		10
4	Timing analysis considering temporal supply voltage fluctuation **2005**,		10
3	Capturing crosstalk-induced waveform for accurate static timing analysis **2003**,		8
2	Crosstalk noise optimization by post-layout transistor sizing **2002**,		10
1	Via-switch FPGA with transistor-free programmability enabling energy-efficient near-memory parallel computation. *Japanese Journal of Applied Physics*,	1.4	0