

Ashok Srivastava

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Ternary input signal to binary bit output conversion CMOS integrated circuit design using neuron MOSFETs. <i>Microsystem Technologies</i> , 2022, 28, 101-108.	2.0	2
2	Evaluating the Performances of Memristor, FinFET, and Graphene TFET in VLSI Circuit Design. , 2021, , .		13
3	An Ultra-Low Power MOS2 Tunnel Field Effect Transistor PLL Design for IoT Applications. , 2021, , .		7
4	Phase Noise and Jitter Measurements in SEU-Hardened CMOS Phase Locked Loop Design. , 2021, , .		8
5	High Q-Factor Graphene-Based Inductor CMOS LC Voltage Controlled Oscillator for PLL Applications. , 2021, , .		1
6	Analytical Current Transport Modeling of Monolayer Molybdenum Disulfide-Based Dual Gate Tunnel Field Effect Transistor. <i>IEEE Nanotechnology Magazine</i> , 2020, 19, 620-627.	2.0	16
7	0.4ÂmW, 0.27 pJ/bit true random number generator using jitter, metastability and current starved topology. <i>IET Circuits, Devices and Systems</i> , 2020, 14, 1001-1011.	1.4	3
8	A 250 MHz-to-1.6 GHz Phase Locked Loop Design in Hybrid FinFET-Memristor Technology. , 2020, , .		9
9	Memristor-Based Loop Filter Design for Phase Locked Loop. <i>Journal of Low Power Electronics and Applications</i> , 2019, 9, 24.	2.0	16
10	Synthesis of Two-Dimensional Diamond From Graphene on Copper. , 2019, , .		1
11	Computational study of silicene nanoribbon tunnel field-effect transistor. <i>Microsystem Technologies</i> , 2019, , 1.	2.0	3
12	Long Short-Term Memory Network Design for Analog Computing. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , 2019, 15, 1-27.	2.3	33
13	qSwitch: Dynamical Off-Chip Bandwidth Allocation Between Local and Remote Accesses. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018, 37, 75-87.	2.7	2
14	A Multiple Input Floating Gate Based Arithmetic Logic Unit with a Feedback Loop for Digital Calibration. <i>Journal of Low Power Electronics</i> , 2018, 14, 535-547.	0.6	2
15	Evaluation of Four Power Gating Schemes Applied to ECRL Adiabatic Logic. , 2018, , .		2
16	SPICE-Compatible Modeling of Silicene Field Effect Transistor and Analog Circuit Design. , 2018, , .		0
17	Calibration method to reduce the error in logarithmic conversion with its circuit implementation. <i>IET Circuits, Devices and Systems</i> , 2018, 12, 301-308.	1.4	1
18	Using Switchable Pins to Increase Off-Chip Bandwidth in Chip-Multiprocessors. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2017, 28, 274-289.	5.6	3

#	ARTICLE	IF	CITATIONS
19	A novel switchable pin method for regulating power in chip-multiprocessor. The Integration VLSI Journal, 2017, 58, 329-338.	2.1	0
20	Modeling of Joule Heating Induced Effects in Multiwall Carbon Nanotube Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3089-3098.	3.1	8
21	Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design. , 2017, , .		0
22	Subthreshold Slope of Vertical Graphene Interlayer Tunnel Transistor. Nano, 2017, 12, 1750069.	1.0	0
23	Effect of Edge Roughness on Static Characteristics of Graphene Nanoribbon Field Effect Transistor. Electronics (Switzerland), 2016, 5, 11.	3.1	14
24	Transport Phenomenon in Boron-Group V Linear Atomic Chains Under Tensile Stress for Nanoscale Devices and Interconnects: First Principles Analysis. IEEE Transactions on Electron Devices, 2016, 63, 4899-4906.	3.0	8
25	Modeling of Graphene Nanoribbon Tunnel Field Effect Transistor in Verilog-A for Digital Circuit Design. , 2016, , .		7
26	Width-Dependent Characteristics of Graphene Nanoribbon Field Effect Transistor for High Frequency Applications. , 2016, , .		1
27	Vertical MoS ₂ / h BN/MoS ₂ interlayer tunneling field effect transistor. Solid-State Electronics, 2016, 126, 96-103.	1.4	21
28	A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic. , 2016, , .		2
29	Analytical Current Transport Modeling of Graphene Nanoribbon Tunnel Field-Effect Transistors for Digital Circuit Design. IEEE Nanotechnology Magazine, 2016, 15, 39-50.	2.0	34
30	A Graphene Switching Transistor for Vertical Circuit Design. ECS Journal of Solid State Science and Technology, 2016, 5, M13-M21.	1.8	4
31	Clocked Adiabatic XOR and XNOR CMOS Gates Design Based on Graphene Nanoribbon Complementary Field Effect Transistors. , 2015, , .		0
32	Circuit Implementation of Switchable Pins in Chip Multiprocessor. , 2015, , .		2
33	An Algorithm Used in a Power Monitor to Mitigate Dark Silicon on VLSI Chip. , 2015, , .		1
34	Characterization of SWCNT Bundle Based VLSI Interconnect with Self-heating Induced Scatterings. , 2015, , .		5
35	Powering Up Dark Silicon: Mitigating the Limitation of Power Delivery via Dynamic Pin Switching. IEEE Transactions on Emerging Topics in Computing, 2015, 3, 489-501.	4.6	4
36	Increasing off-chip bandwidth in multi-core processors with switchable pins. , 2014, , .		6

#	ARTICLE	IF	CITATIONS
37	Characterization of MWCNT VLSI Interconnect with Self-Heating Induced Scatterings. , 2014, , .		5
38	A novel graphene nanoribbon field effect transistor for integrated circuit design. , 2013, , .		13
39	A Thermal Model for Carbon Nanotube Interconnects. Nanomaterials, 2013, 3, 229-241.	4.1	22
40	Testing of Trusted CMOS Data Converters. , 2012, , .		0
41	Emerging Carbon Nanotube Electronic Circuits, Modeling, and Performance. VLSI Design, 2010, 2010, 1-8.	0.5	6
42	Carbon nanotubes for next generation very large scale integration interconnects. Journal of Nanophotonics, 2010, 4, 041690.	1.0	42
43	Combined oscillation and I DDQ testing of a CMOS amplifier circuit. International Journal of Electronics, 2010, 97, 1-15.	1.4	3
44	A model of multi-walled carbon nanotube interconnects. , 2009, , .		8
45	Current transport modeling of carbon nanotube field effect transistors. Physica Status Solidi (A) Applications and Materials Science, 2009, 206, 1569-1578.	1.8	19
46	Carrier density and effective mass calculations in carbon nanotubes. Physica Status Solidi (B): Basic Research, 2008, 245, 2558-2562.	1.5	61
47	Numerical Modeling of the I-V Characteristic of Carbon Nanotube Field Effect Transistors (CNT-FETs). System Theory, Proceedings of the Southeastern Symposium on, 2008, , .	0.0	7
48	THRESHOLD AND SATURATION VOLTAGES MODELING OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNT-FETs). Nano, 2008, 03, 195-201.	1.0	10
49	An Adaptive Body-Bias Generator for Low Voltage CMOS VLSI Circuits. International Journal of Distributed Sensor Networks, 2008, 4, 213-222.	2.2	16
50	Δl&sub&DDQ&/sub& testing of a 12-bit recycling architecture based ADC. , 2007, , .		0
51	Hot Carrier Effects in Wireless Communication Systems Built on Short-Channel MOSFETs. IEEE Transactions on Wireless Communications, 2007, 6, 2402-2406.	9.2	2
52	Carrier Density and Effective Mass Calculations for Carbon Nanotubes. , 2007, , .		5
53	An Experimental Study of Phase Noise in CMOS Phase-Locked Loops Considering Different Noise Sources. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	0
54	HOT CARRIER EFFECTS ON JITTER PERFORMANCE IN CMOS VOLTAGE-CONTROLLED OSCILLATORS. Fluctuation and Noise Letters, 2006, 06, L329-L334.	1.5	6

#	ARTICLE	IF	CITATIONS
55	Delta-I _{DDQ} Testing of a CMOS 12-Bit Charge Scaling DigitaltoAnalog Converter. , 2006, , .		3
56	A comparator-based I _{DDQ} testing of CMOS analog and mixed-signal integrated circuits. , 2005, , .		2
57	<title>Novel scheme for a higher bandwidth sensor readout</title>. , 2002, , .		5