Ashok Srivastava

List of Publications by Year
in descending order

57	475	840776 11	839539 18
papers	citations	h-index	g-index

58	58	58	431
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Carrier density and effective mass calculations in carbon nanotubes. Physica Status Solidi (B): Basic Research, 2008, 245, 2558-2562.	1.5	61
2	Carbon nanotubes for next generation very large scale integration interconnects. Journal of Nanophotonics, 2010, 4, 041690.	1.0	42
3	Analytical Current Transport Modeling of Graphene Nanoribbon Tunnel Field-Effect Transistors for Digital Circuit Design. IEEE Nanotechnology Magazine, 2016, 15, 39-50.	2.0	34
4	Long Short-Term Memory Network Design for Analog Computing. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-27.	2.3	33
5	A Thermal Model for Carbon Nanotube Interconnects. Nanomaterials, 2013, 3, 229-241.	4.1	22
6	Vertical MoS 2 / h BN/MoS 2 interlayer tunneling field effect transistor. Solid-State Electronics, 2016, 126, 96-103.	1.4	21
7	Current transport modeling of carbon nanotube field effect transistors. Physica Status Solidi (A) Applications and Materials Science, 2009, 206, 1569-1578.	1.8	19
8	An Adaptive Body-Bias Generator for Low Voltage CMOS VLSI Circuits. International Journal of Distributed Sensor Networks, 2008, 4, 213-222.	2.2	16
9	Memristor-Based Loop Filter Design for Phase Locked Loop. Journal of Low Power Electronics and Applications, 2019, 9, 24.	2.0	16
10	Analytical Current Transport Modeling of Monolayer Molybdenum Disulfide-Based Dual Gate Tunnel Field Effect Transistor. IEEE Nanotechnology Magazine, 2020, 19, 620-627.	2.0	16
11	Effect of Edge Roughness on Static Characteristics of Graphene Nanoribbon Field Effect Transistor. Electronics (Switzerland), 2016, 5, 11.	3.1	14
12	A novel graphene nanoribbon field effect transistor for integrated circuit design. , 2013, , .		13
13	Evaluating the Performances of Memristor, FinFET, and Graphene TFET in VLSI Circuit Design. , 2021, , .		13
14	THRESHOLD AND SATURATION VOLTAGES MODELING OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNT-FETs). Nano, 2008, 03, 195-201.	1.0	10
15	A 250 MHz-to-1.6 GHz Phase Locked Loop Design in Hybrid FinFET-Memristor Technology. , 2020, , .		9
16	A model of multi-walled carbon nanotube interconnects. , 2009, , .		8
17	Transport Phenomenon in Boronâ€“GroupV Linear Atomic Chains Under Tensile Stress for Nanoscale Devices and Interconnects: First Principles Analysis. IEEE Transactions on Electron Devices, 2016, 63, 4899-4906.	3.0	8
18	Modeling of Joule Heating Induced Effects in Multiwall Carbon Nanotube Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3089-3098.	3.1	8

#	Article	IF	Citations
19	Phase Noise and Jitter Measurements in SEU-Hardened CMOS Phase Locked Loop Design. , 2021, , .		8
20	Numerical Modeling of the I-V Characteristic of Carbon Nanotube Field Effect Transistors (CNT-FETs). System Theory, Proceedings of the Southeastern Symposium on, 2008, , .	0.0	7
21	Modeling of Graphene Nanoribbon Tunnel Field Effect Transistor in Verilog-A for Digital Circuit Design. , 2016, , .		7
22	An Ultra-Low Power MOS2 Tunnel Field Effect Transistor PLL Design for IoT Applications. , 2021, , .		7
23	HOT CARRIER EFFECTS ON JITTER PERFORMANCE IN CMOS VOLTAGE-CONTROLLED OSCILLATORS. Fluctuation and Noise Letters, 2006, 06, L329-L334.	1.5	6
24	Emerging Carbon Nanotube Electronic Circuits, Modeling, and Performance. VLSI Design, 2010, 2010, 1-8.	0.5	6
25	Increasing off-chip bandwidth in multi-core processors with switchable pins. , 2014, , .		6
26	<title>Novel scheme for a higher bandwidth sensor readout</title>. , 2002, , .		5
27	Carrier Density and Effective Mass Calculations for Carbon Nanotubes. , 2007, , .		5
28	Characterization of MWCNT VLSI Interconnect with Self-Heating Induced Scatterings. , 2014, , .		5
29	Characterization of SWCNT Bundle Based VLSI Interconnect with Self-heating Induced Scatterings. , 2015, , .		5
30	Powering Up Dark Silicon: Mitigating the Limitation of Power Delivery via Dynamic Pin Switching. IEEE Transactions on Emerging Topics in Computing, 2015, 3, 489-501.	4.6	4
31	A Graphene Switching Transistor for Vertical Circuit Design. ECS Journal of Solid State Science and Technology, 2016, 5, M13-M21.	1.8	4
32	Delta-I_{DDQ} Testing of a CMOS 12-Bit Charge Scaling DigitaltoAnalog Converter. , 2006, , .		3
33	Combined oscillation and I DDQ testing of a CMOS amplifier circuit. International Journal of Electronics, 2010, 97, 1-15.	1.4	3
34	Using Switchable Pins to Increase Off-Chip Bandwidth in Chip-Multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 274-289.	5.6	3
35	Computational study of silicene nanoribbon tunnel field-effect transistor. Microsystem Technologies, 2019, , 1.	2.0	3
36	0.4ÂmW, 0.27 pJ/bit true random number generator using jitter, metastability and current starved topology. IET Circuits, Devices and Systems, 2020, 14, 1001-1011.	1.4	3

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37	A comparator-based I/sub DDQ/ testing of CMOS analog and mixed-signal integrated circuits. , 2005, , .		2
38	Hot Carrier Effects in Wireless Communication Systems Built on Short-Channel MOSFETs. IEEE Transactions on Wireless Communications, 2007, 6, 2402-2406.	9.2	2
39	Circuit Implementation of Switchable Pins in Chip Multiprocessor. , 2015, , .		2
40	A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic. , 2016, , .		2
41	qSwitch: Dynamical Off-Chip Bandwidth Allocation Between Local and Remote Accesses. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 75-87.	2.7	2
42	A Multiple Input Floating Gate Based Arithmetic Logic Unit with a Feedback Loop for Digital Calibration. Journal of Low Power Electronics, 2018, 14, 535-547.	0.6	2
43	Evaluation of Four Power Gating Schemes Applied to ECRL Adiabatic Logic. , 2018, , .		2
44	Ternary input signal to binary bit output conversion CMOS integrated circuit design using neuron MOSFETs. Microsystem Technologies, 2022, 28, 101-108.	2.0	2
45	An Algorithm Used in a Power Monitor to Mitigate Dark Silicon on VLSI Chip. , 2015, , .		1
46	Width-Dependent Characteristics of Graphene Nanoribbon Field Effect Transistor for High Frequency Applications. , 2016, , .		1
47	Calibration method to reduce the error in logarithmic conversion with its circuit implementation. IET Circuits, Devices and Systems, 2018, 12, 301-308.	1.4	1
48	Synthesis of Two-Dimensional Diamond From Graphene on Copper. , 2019, , .		1
49	High Q-Factor Graphene-Based Inductor CMOS LC Voltage Controlled Oscillator for PLL Applications. , 2021, , .		1
50	An Experimental Study of Phase Noise in CMOS Phase-Locked Loops Considering Different Noise Sources. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	0
51	ΔI_{DDQ} testing of a 12-bit recycling architecture based ADC. , 2007, , .		0
52	Testing of Trusted CMOS Data Converters. , 2012, , .		0
53	Clocked Adiabatic XOR and XNOR CMOS Gates Design Based on Graphene Nanoribbon Complementary Field Effect Transistors. , 2015, , .		0
54	A novel switchable pin method for regulating power in chip-multiprocessor. The Integration VLSI Journal, 2017, 58, 329-338.	2.1	0

#	Article	IF	Citations
55	Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design. , 2017, , .		0
56	Subthreshold Slope of Vertical Graphene Interlayer Tunnel Transistor. Nano, 2017, 12, 1750069.	1.0	0
57	SPICE-Compatible Modeling of Silicene Field Effect Transistor and Analog Circuit Design. , 2018, , .		0