

Frank Mueller

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/2518231/publications.pdf>

Version: 2024-02-01

84
papers

3,153
citations

516215

16
h-index

329751

37
g-index

85
all docs

85
docs citations

85
times ranked

1702
citing authors

#	ARTICLE	IF	CITATIONS
1	CLAIRE: Enabling Continual Learning for Real-time Autonomous Driving with a Dual-head Architecture. , 2022, , .		2
2	Hummingbird: efficient performance prediction for executing genomic applications in the cloud. Bioinformatics, 2021, 37, 2537-2543.	1.8	4
3	NUMA-aware memory coloring for multicore real-time systems. Journal of Systems Architecture, 2021, 118, 102188.	2.5	2
4	Mapping Constraint Problems onto Quantum Gate and Annealing Devices. , 2021, , .		1
5	BarrierFinder: recognizing ad hoc barriers. Empirical Software Engineering, 2020, 25, 4676-4706.	3.0	0
6	Implementing NChooseK on IBM Q Quantum Computer Systems. Lecture Notes in Computer Science, 2019, , 209-223.	1.0	2
7	FancyTuner. , 2019, , .		4
8	End-to-End Resilience for HPC Applications. Lecture Notes in Computer Science, 2019, , 271-290.	1.0	1
9	BARRIERFINDER: Recognizing Ad Hoc Barriers. , 2019, , .		1
10	Automatically Translating Quantum Programs from a Subset of Common Gates to an Adiabatic Representation. Lecture Notes in Computer Science, 2019, , 146-161.	1.0	0
11	Controller-aware memory coloring for multicore real-time systems. , 2018, , .		8
12	Chameleon: Online Clustering of MPI Program Traces. , 2018, , .		2
13	A Failure Recovery Protocol for Software-Defined Real-Time Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2222-2232.	1.9	2
14	Co-Scheduling on Fused CPU-GPU Architectures With Shared Last Level Caches. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2337-2347.	1.9	6
15	DINO: Divergent node cloning for sustained redundancy in HPC. Journal of Parallel and Distributed Computing, 2017, 109, 350-362.	2.7	3
16	Scalable communication event tracing via clustering. Journal of Parallel and Distributed Computing, 2017, 109, 230-244.	2.7	5
17	ScalaIOExtrap: Elastic I/O Tracing and Extrapolation. , 2017, , .		6
18	TintMalloc: Reducing Memory Access Divergence via Controller-Aware Coloring. , 2016, , .		11

#	ARTICLE	IF	CITATIONS
19	Benchmark Generation and Simulation at Extreme Scale. , 2016, , .		1
20	FlipSphere: A Software-Based DRAM Error Detection and Correction Library for HPC. , 2016, , .		5
21	SparkScore: Leveraging Apache Spark for Distributed Genomic Inference. , 2016, , .		6
22	Efficient clustering for ultra-scale application tracing. Journal of Parallel and Distributed Computing, 2016, 98, 25-39.	2.7	8
23	ACURDION: An adaptive clustering-based algorithm for tracing large-scale MPI applications. , 2015, , .		2
24	OpenACC acceleration of an unstructured CFD solver based on a reconstructed discontinuous Galerkin method for compressible flows. International Journal for Numerical Methods in Fluids, 2015, 78, 123-139.	0.9	21
25	Architecture aware semi partitioned real-time scheduling on multicore platforms. Real-Time Systems, 2015, 51, 274-313.	1.1	4
26	Providing task isolation via TLB coloring. , 2015, , .		14
27	Intrusion Detection for CPS Real-Time Controllers. Power Systems, 2015, , 329-358.	0.3	7
28	Scalable performance analysis of exascale MPI programs through signature-based clustering algorithms. , 2014, , .		7
29	Exploiting Data Representation for Fault Tolerance. , 2014, , .		3
30	Evaluating the Impact of SDC on the GMRES Iterative Solver. , 2014, , .		58
31	Understanding the tradeoffs between software-managed vs. hardware-managed caches in GPUs. , 2014, , .		22
32	Autogeneration and Autotuning of 3D Stencil Codes on Homogeneous and Heterogeneous GPU Clusters. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 417-427.	4.0	28
33	Elastic and scalable tracing and accurate replay of non-deterministic events. , 2013, , .		30
34	Sustained Resilience via Live Process Cloning. , 2013, , .		3
35	S <sc>cala</sc> E <sc>xtrap</sc>. ACM Transactions on Programming Languages and Systems, 2012, 34, 1-29.	1.7	14
36	Combining Partial Redundancy and Checkpointing for HPC. , 2012, , .		95

#	ARTICLE	IF	CITATIONS
37	Fault Resilient Real-Time Design for NoC Architectures. , 2012, , .		3
38	ScalaBenchGen: Auto-Generation of Communication Benchmarks Traces. , 2012, , .		18
39	Semi-Partitioned Hard-Real-Time Scheduling under Locked Cache Migration in Multicore Systems. , 2012, , .		21
40	Probabilistic Communication and I/O Tracing with Deterministic Replay at Scale. , 2011, , .		25
41	GStream: A General-Purpose Data Streaming Framework on GPU Clusters. , 2011, , .		20
42	Making DRAM refresh predictable. Real-Time Systems, 2011, 47, 430-453.	1.1	27
43	Data-intensive document clustering on graphics processing unit (GPU) clusters. Journal of Parallel and Distributed Computing, 2011, 71, 211-224.	2.7	20
44	Automatic Generation of Executable Communication Specifications from Parallel Applications. , 2011, , .		1
45	Predictable task migration for locked caches in multi-core systems. , 2011, , .		19
46	Feedback-directed page placement for ccNUMA via hardware-generated memory traces. Journal of Parallel and Distributed Computing, 2010, 70, 1204-1219.	2.7	38
47	Parametric timing analysis and its application to dynamic voltage scaling. Transactions on Embedded Computing Systems, 2010, 10, 1-34.	2.1	6
48	Tightening the bounds on feasible preemptions. Transactions on Embedded Computing Systems, 2010, 10, 1-34.	2.1	26
49	Large-scale multi-dimensional document clustering on GPU clusters. , 2010, , .		15
50	Hybrid Checkpointing for MPI Jobs in HPC Environments. , 2010, , .		29
51	Fault Tolerant Network Routing through Software Overlays for Intelligent Power Grids. , 2010, , .		7
52	Push-assisted migration of real-time tasks in multi-core processors. ACM SIGPLAN Notices, 2009, 44, 80-89.	0.2	12
53	Improving the availability of supercomputer job input data using temporal replication. Computer Science - Research and Development, 2009, 23, 149-157.	2.7	6
54	ScalaTrace: Scalable compression and replay of communication traces for high-performance computing. Journal of Parallel and Distributed Computing, 2009, 69, 696-710.	2.7	223

#	ARTICLE	IF	CITATIONS
55	Bounding Worst-Case Response Times of Tasks under PIP. , 2009, , .		0
56	Push-assisted migration of real-time tasks in multi-core processors. , 2009, , .		20
57	The worst-case execution-time problem“ overview of methods and survey of tools. Transactions on Embedded Computing Systems, 2008, 7, 1-53.	2.1	1,293
58	Proactive process-level live migration in HPC environments. , 2008, , .		6
59	Merging State and Preserving Timing Anomalies in Pipelines of High-End Processors. , 2008, , .		9
60	Bounding Worst-Case Response Time for Tasks with Non-Preemptive Regions. , 2008, , .		20
61	On-the-Fly Recovery of Job Input Data in Supercomputers. , 2008, , .		0
62	Hybrid Timing Analysis of Modern Processor Pipelines via Hardware/Software Interactions. , 2008, , .		7
63	Optimizing center performance through coordinated data staging, scheduling and recovery. , 2007, , .		21
64	A Job Pause Service under LAM/MPI+BLCR for Transparent Fault Tolerance. , 2007, , .		54
65	METRIC. ACM Transactions on Programming Languages and Systems, 2007, 29, 12.	1.7	21
66	Scalable Compression and Replay of Communication Traces in Massively P arallel E nvironments. , 2007, , .		28
67	Source-Code-Related Cache Coherence Characterization of OpenMP Benchmarks. IEEE Transactions on Parallel and Distributed Systems, 2007, 18, 818-834.	4.0	8
68	Improving WCET by applying worst-case path optimizations. Real-Time Systems, 2006, 34, 129-152.	1.1	9
69	Hardware profile-guided automatic page placement for ccNUMA systems. , 2006, , .		52
70	FAST. Transactions on Embedded Computing Systems, 2006, 5, 200-224.	2.1	34
71	Analysis of cache-coherence bottlenecks with hybrid hardware/software techniques. Transactions on Architecture and Code Optimization, 2006, 3, 390-423.	1.6	9
72	Feedback EDF Scheduling of Real-Time Tasks Exploiting Dynamic Voltage Scaling. Real-Time Systems, 2005, 31, 33-63.	1.1	52

#	ARTICLE	IF	CITATIONS
73	Improving WCET by applying a WC code-positioning optimization. Transactions on Architecture and Code Optimization, 2005, 2, 335-365.	1.6	25
74	A hybrid hardware/software approach to efficiently determine cache coherence Bottlenecks. , 2005, , .		11
75	Compositional static instruction cache simulation. ACM SIGPLAN Notices, 2004, 39, 136-145.	0.2	1
76	Communication characteristics of large-scale scientific applications for contemporary cluster architectures. Journal of Parallel and Distributed Computing, 2003, 63, 853-865.	2.7	94
77	Virtual simple architecture (VISA). Computer Architecture News, 2003, 31, 350-361.	2.5	3
78	Energy-conserving feedback EDF scheduling for embedded systems with real-time constraints. , 2002, , .		37
79	Energy-conserving feedback EDF scheduling for embedded systems with real-time constraints. ACM SIGPLAN Notices, 2002, 37, 213-222.	0.2	7
80	A Comparison of Static Analysis and Evolutionary Testing for the Verification of Timing Constraints. Real-Time Systems, 2001, 21, 241-268.	1.1	99
81	Timing Analysis for Instruction Caches. Real-Time Systems, 2000, 18, 217-247.	1.1	129
82	Timing Analysis for Data and Wrap-Around Fill Caches. Real-Time Systems, 1999, 17, 209-233.	1.1	38
83	Avoiding conditional branches by code replication. , 1995, , .		54
84	Avoiding unconditional jumps by code replication. , 1992, , .		37