Armin Tajalli

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/2501082/publications.pdf

Version: 2024-02-01

69	653	840585	713332
papers	citations	11	21
		h-index	g-index

72	72	72	458
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Subthreshold Source-Coupled Logic Circuits for Ultra-Low-Power Applications. IEEE Journal of Solid-State Circuits, 2008, 43, 1699-1710.	3.5	91
2	A Review on Quantum Computing: From Qubits to Front-end Electronics and Cryogenic MOSFET Physics. , 2019, , .		57
3	Design Trade-offs in Ultra-Low-Power Digital Nanoscale CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2189-2200.	3.5	55
4	A Slew Controlled LVDS Output Driver Circuit in 0.18 mum CMOS Technology. IEEE Journal of Solid-State Circuits, 2009, 44, 538-548.	3.5	50
5	Extreme Low-Power Mixed Signal IC Design. , 2010, , .		42
6	A 1.02-pJ/b 20.83-Gb/s/Wire USR Transceiver Using CNRZ-5 in 16-nm FinFET. IEEE Journal of Solid-State Circuits, 2020, 55, 1108-1123.	3.5	27
7	Hybrid NRZ/Multi-Tone Serial Data Transceiver for Multi-Drop Memory Interfaces. IEEE Journal of Solid-State Circuits, 2015, 50, 3133-3144.	3.5	24
8	Ultra low power subthreshold MOS current mode logic circuits using a novel load device concept. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2007, , .	0.0	23
9	Leakage Current Reduction Using Subthreshold Source-Coupled Logic. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 374-378.	2.2	20
10	Improving Power-Delay Performance of Ultra-Low-Power Subthreshold SCL Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 127-131.	2.2	20
11	Low-Power and Widely Tunable Linearized Biquadratic Low-Pass Transconductor-C Filter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 159-163.	2.2	17
12	A Power-Efficient Clock and Data Recovery Circuit in 0.18 $mu{hbox {m}}$ CMOS Technology for Multi-Channel Short-Haul Optical Data Communication. IEEE Journal of Solid-State Circuits, 2007, 42, 2235-2244.	3.5	16
13	Subthreshold SCL for ultra-low-power SRAM and low-activity-rate digital systems. , 2009, , .		13
14	Analysis and Characterization of Variability in Subthreshold Source-Coupled Logic Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 458-467.	3.5	13
15	10.3 A 7.5mW 7.5Gb/s mixed NRZ/multi-tone serial-data transceiver for multi-drop memory interfaces in 40nm CMOS. , 2015, , .		12
16	Power-Speed Trade-Offs in Design of Scaled FET Circuits Using C/I _{DS} Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 631-640.	3.5	12
17	Chord Signaling for High-Speed Data Movement: Employing Advanced Communication and Circuit Techniques to Augment Data-Transfer Bandwidth. IEEE Solid-State Circuits Magazine, 2019, 11, 78-85.	0.5	11
18	Ultra-low power 32-bit pipelined adder using subthreshold source-coupled logic with 5fJ/stage PDP. Microelectronics Journal, 2009, 40, 973-978.	1.1	9

#	Article	IF	Citations
19	Improving the power-delay product in SCL circuits using source follower output stage. , 2008, , .		8
20	A widely-tunable and ultra-low-power MOSFET-C filter operating in subthreshold. , 2009, , .		8
21	An area and power optimization technique for CMOS bandgap voltage references. Analog Integrated Circuits and Signal Processing, 2010, 62, 131-140.	0.9	8
22	A 32-Gb/s PAM-4 SST Transmitter With Four-Tap FFE Using High-Impedance Driver in 28-nm FDSOI. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1132-1140.	2.1	7
23	The Sensitivity of ENRZ to Crosstalk - In Comparison to NRZ, PAM3, and PAM4. , 2021, , .		7
24	A 9 pW/Hz adjustable clock generator with 3-decade tuning range for dynamic power management in subthreshold SCL systems. , 2010, , .		6
25	Power and area efficient MOSFET-C filter for very low frequency applications. Analog Integrated Circuits and Signal Processing, 2012, 70, 123-132.	0.9	6
26	CMOS Amplifier Design Based on Extended g_{m}/I_{D} Methodology. , 2019, , .		6
27	A Low-Power 10 to 15 Gb/s Common-Gate CTLE Based on Optimized Active Inductors. , 2020, , .		6
28	Link Performance Comparison based on Insertion Loss: NRZ, PAM3, PAM4, and ENRZ. , 2020, , .		6
29	A Wide Tuning Range, Fractional Multiplying Delay-Locked Loop Topology for Frequency Hopping Applications. Analog Integrated Circuits and Signal Processing, 2006, 46, 203-214.	0.9	5
30	A power-efficient LVDS driver circuit in 0.18-Î¼m CMOS technology. , 2007, , .		5
31	Ultra-low power mixed-signal design platform using subthreshold source-coupled circuits. , 2010, , .		5
32	Subthreshold current-mode oscillator-based quantizer with 3-decade scalable sampling rate and pico-Ampere range resolution. , 2010, , .		5
33	Matrix phase detector for high bandwidth and low jitter frequency synthesis. Electronics Letters, 2017, 53, 1031-1033.	0.5	5
34	Multi-Stage Current-Steering Amplifier Design Based on Extended g_m/I_D Methodology. , 2019, , .		5
35	Nanowatt Range Folding-Interpolating Analog-to-Digital Converter Using Subthreshold Source-Coupled Circuits. Journal of Low Power Electronics, 2010, 6, 211-217.	0.6	4
36	Subthreshold leakage reduction: A comparative study of SCL and CMOS design. , 2009, , .		3

#	Article	IF	Citations
37	Wide-Range Dynamic Power Management in Low-Voltage Low-Power Subthreshold SCL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 903-907.	2.2	3
38	A subthreshold currentâ€sensing Î£Î" modulator for lowâ€voltage and lowâ€power sensor interfaces. International Journal of Circuit Theory and Applications, 2015, 43, 1597-1614.	1.3	3
39	A Digital Spectrum Shaping Signaling Serial-Data Transceiver With Crosstalk and ISI Reduction Property in Multidrop Interfaces. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 1126-1130.	2.2	3
40	A Time-Division Multiplexing Signaling Scheme for Inter-Symbol/Channel Interference Reduction in Low-Power Multi-Drop Memory Links. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1387-1391.	2.2	3
41	Power System Emulator Based on PLL Architecture. , 2020, , .		3
42	Short-Reach and Pin-Efficient Interfaces Using Correlated NRZ. , 2020, , .		3
43	Systematic Design of Loop Circuit Topologies Using C/I _{DS} Methodology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1538-1542.	2.1	3
44	A 4×9 Gb/s 1 pJ/b NRZ/multi-tone serial-data transceiver with crosstalk reduction architecture for multi-drop memory interfaces in 40nm CMOS. , 2015, , .		2
45	ISI Sensitivity of PAM Signaling for Very High-Speed Short-Reach Copper Links. , 2019, , .		2
46	Subthreshold Source-Coupled Logic. , 2010, , 61-97.		2
47	A Subthreshold SCL Based Pipelined Encoder for Ultra-Low Power 8-bit Folding/Interpolating ADC. , 2008, , .		1
48	Design trade-offs in ultra-low-power CMOS and STSCL digital systems. , 2011, , .		1
49	A 10b SAR ADC with Widely Scalable Sampling Rate and AGC Amplifier Front-End. , 2018, , .		1
50	Spectrum-Efficient Communication Over Copper Using Hybrid Amplitude and Spatial Signaling. , 2019, , .		1
51	Digitally-Assisted Peak Detector for Periodic Signal. , 2020, , .		1
52	Optimal PAM Order for Wireline Communication. , 2021, , .		1
53	Energy and Area Efficient Mixed-Mode MCMC MIMO Detector. , 2020, , .		1
54	Improving the Power-Delay Performance in Subthreshold Source-Coupled Logic Circuits. Lecture Notes in Computer Science, 2009, , 21-30.	1.0	1

#	Article	IF	Citations
55	Low-Voltage CMOS Transconductor-C Filter Design Using Charge-Pump Circuit. Analog Integrated Circuits and Signal Processing, 2005, 44, 219-229.	0.9	0
56	Structured Design of Integrated Subscriber Line Interface System and Circuit. Analog Integrated Circuits and Signal Processing, 2005, 45, 47-59.	0.9	0
57	A Low Power Base-Band Circuit for Low-IF Wireless PAN Receivers. , 2006, , .		0
58	A Power Optimized Base-Band Circuitry for the Low-IF Receivers. , 2007, , .		0
59	A 5.43-μW 0.8-V subthreshold current-sensing ΣΔ modulator for low-noise sensor interfaces. , 2014, , .		0
60	Mixed-Mode Signal Processing for Implementing MCMC MIMO Detector. IFIP Advances in Information and Communication Technology, 2021, , 21-37.	0.5	0
61	Tradeoffs in Design of Low-Power Gated-Oscillator Clock and Data Recovery Circuits. Journal of Low Power Electronics, 2007, 3, 345-354.	0.6	0
62	Widely Adjustable Ring Oscillator Based Î£Î” ADC. , 2010, , 215-242.		0
63	Widely Adjustable Continuous-Time Filter Design. , 2010, , 161-185.		0
64	Low-Activity-Rate and Memory Circuits in STSCL. , 2010, , 141-158.		0
65	Subthreshold MOS for Ultra-Low Power. , 2010, , 15-58.		0
66	Scalable Folding and Interpolating ADC Design. , 2010, , 187-213.		0
67	Subthreshold Source-Coupled Logic Performance Analysis. , 2010, , 115-139.		0
68	STSCL Standard Cell Library Development. , 2010, , 99-113.		0
69	Wide Tuning Range PLL. , 2010, , 243-259.		0