Rishu Chaujar

List of Publications by Year
in descending order

194	2,307	218677	289244
papers	citations	26 h-index	40 g-index

196	196	196	725
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Design and Investigation of Recessed-T-Gate Double Channel HEMT with InGaN Back Barrier for Enhanced Performance. Arabian Journal for Science and Engineering, 2022, 47, 1109-1116.	3.0	12
2	Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance. Silicon, 2022, 14, 309-321.	3.3	16
3	TCAD investigation of ferroelectric based substrate MOSFET for digital application. Silicon, 2022, 14, 5075-5084.	3.3	10
4	Numerical simulation of analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for ULSI switching applications. European Physical Journal Plus, 2022, 137, 1.	2.6	6
5	Ultrascaled 10Ânm Tâ€gate Eâ€mode <scp>InAlN</scp> / <scp>AlN HEMT</scp> with polarized doped buffer for high power microwave applications. International Journal of RF and Microwave Computer-Aided Engineering, 2022, 32, .	1.2	8
6	Influence of source electrode metal work function on polar gate prompted source hole plasma in arsenide/antimonide tunneling interfaced junctionless TFET. Journal of Micromechanics and Microengineering, 2022, 32, 044004.	2.6	2
7	Sensitivity Analysis of Biomolecule Nanocavity Immobilization in a Dielectric Modulated Triple-Hybrid Metal Gate-All-Around Junctionless NWFET Biosensor for Detecting Various Diseases. Journal of Electronic Materials, 2022, 51, 2236-2247.	2.2	11
8	RF, linearity and intermodulation distortion analysis with small-signal parameters extraction of tunable bandgap arsenide/antimonide tunneling interfaced JLTFET. Microsystem Technologies, 2022, 28, 2659-2667.	2.0	3
9	Compatibility of a Truncated Fin-FinFET as a k-modulated Biosensor with Optimum parameters for Pre-emptive Diagnosis of Diseases. Computers and Electrical Engineering, 2022, 100, 107850.	4.8	0
10	Quantum ATK analysis of silicon nanowire FET with a cylindrical metallic wrap-around gate varied with dielectrics. Materials Today: Proceedings, 2022, 62, 3823-3826.	1.8	0
11	Detection of biomolecules in dielectric modulated double metal below ferroelectric layer FET with improved sensitivity. Journal of Materials Science: Materials in Electronics, 2022, 33, 13558-13567.	2.2	6
12	Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer. Silicon, 2022, 14, 12269-12280.	3.3	8
13	Numerical investigation and temperature-based analysis of the analog performance of fully gate-covered junctionless FinFET. Computers and Electrical Engineering, 2022, 101, 108071.	4.8	2
14	Impact of tunnel gate process variations on analog/radio frequency (microwave) and small signal parameters of heteroâ€material tunneling interfaced charge plasma junctionless tunnel field effect transistor. International Journal of Circuit Theory and Applications, 2022, 50, 3626-3641.	2.0	3
15	RF Analysis of a Fully Gate Covered Junctionless FinFET for Improved Performance. , 2022, , .		0
16	Linearity Performance of Double Metal Negative Capacitance Field-Effect Transistors: A Numerical Study. , 2022, , .		1
17	Reliability of Sub-20Ânm Black Phosphorus Trench (BP-T) MOSFET in High-Temperature Harsh Environment. Silicon, 2021, 13, 1277-1283.	3.3	3
18	Gate Oxide Variability Analysis of a Novel 3 nm Truncated Finâ€“FinFET for High Circuitry Performance. Silicon, 2021, 13, 3249-3256.	3.3	12

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19	Simulation of perovskite solar cell employing ZnO as electron transport layer (ETL) for improved efficiency. Materials Today: Proceedings, 2021, 46, 1684-1687.	1.8	11
20	Interface Trap Charge Analysis of Junctionless Triple Metal Gate High-k Gate All Around Nanowire FET-Based Biotin Biosensor for Detection of Cardiovascular Diseases. Lecture Notes in Electrical Engineering, 2021, , 47-57.	0.4	0
21	A Novel Trench FinFET as a Biosensor for Early Detection of Alzheimerâ€™s Disease. Lecture Notes in Electrical Engineering, 2021, , 35-45.	0.4	0
22	Band gap and gate metal engineering of novel hetero-material InAs/GaAs-based JLTFET for improved wireless applications. Journal of Materials Science: Materials in Electronics, 2021, 32, 3155-3166.	2.2	6
23	Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET. Silicon, 2021, 13, 919-927.	3.3	41
24	Fin Aspect Ratio Optimization of Novel Junctionless Gate Stack Gate All Around (GS-GAA) FinFET for Analog/RF Applications. Lecture Notes in Electrical Engineering, 2021, , 59-67.	0.4	6
25	TCAD Temperature Analysis of Gate Stack Gate All Around (GS-GAA) FinFET for Improved RF and Wireless Performance. Silicon, 2021, 13, 3741-3753.	3.3	32
26	Analysis of a Novel Nanoscale Vacuum Channel TF-FinFET. Silicon, 2021, 13, 3257-3269.	3.3	1
27	Investigation of TF-FinFET Based Biosensor for Early Diagnosis of Protein Carrying Diseases. , 2021, , .		1
28	Recessed Channel Carbon Nanotube Truncated Fin Finfet For High Performance ULSI Applications. , 2021, , .		1
29	Performance enhancement in a novel amalgamation of arsenide/antimonide tunneling interface with charge plasma junctionless-TFET. AEU - International Journal of Electronics and Communications, 2021, 133, 153669.	2.9	14
30	A Comparative Investigation on Characteristics of Conventional MOSFET and Ferroelectric Thin Film Modified FET. , 2021, , .		0
31	Lower Fin Modulation Analysis for a Novel 5nm Top Bottom Gated Junctionless FinFET for improved performance. , 2021, , .		1
32	Investigation of a novel 5nm top bottom gated junctionless FinFET for improved switching and analog performance. Journal of Physics: Conference Series, 2021, 1921, 012100.	0.4	1
33	The Performance Analysis of 70nm T-gate InAlN/AlN MOS-HEMT using Graded Buffer. , 2021, , .		2
34	Technology Computer Aided Design of a Novel Fully Gate Covered Channel Junctionless SOI FinFET for high performance analog application. , 2021, , .		1
35	TCAD Analysis and Simulation of Double Metal Negative Capacitance FET (DM NCFET). , 2021, , .		9
36	Analog Analysis of Novel Ferroelectric-Dual Material Oxide Stack-Double Gate FET. , 2021, , .		0

#	Article	IF	Citations
37	Electrostatic Analysis of Ferroelectric and High Dielectric Layer Assisted MOSFET. , 2021, , .		0
38	Effect of Gate Oxide Material Variability on The Analog Performance of T-Gate GaN-MOS-HEMT with Graded Buffer. , 2021, , .		0
39	A Numerical Study of Analog Parameter of Negative Capacitance Field Effect Transistor with Spacer. , 2021, , .		6
40	Static Performance Assessment of Junctionless Accumulation Mode Gate Stack Gate All Around (JAM-GS-GAA) FinFET Under Severe Temperature. , 2021, , .		0
41	Design Considerations and Capacitance Dependent Parametric Assessment of Gate Metal Engineered SiNW MOSFET for ULSI Switching Applications. Silicon, 2020, 12, 1501-1510.	3.3	5
42	Analysis of structural parameters on sensitivity of black phosphorus junctionless recessed channel MOSFET for biosensing application. Microsystem Technologies, 2020, 26, 2227-2233.	2.0	12
43	Effects of Neural Mechanisms of Pretask Resting EEG Alpha Information on Situational Awareness: A Functional Connectivity Approach. Human Factors, 2020, 62, 1150-1170.	3.5	14
44	Performance evaluation of linearity and intermodulation distortion of nanoscale GaN-SOI FinFET for RFIC design. AEU - International Journal of Electronics and Communications, 2020, 115, 153052.	2.9	31
45	Numerical simulation and parametric assessment of GaN buffered trench gate MOSFET for low power applications. IET Circuits, Devices and Systems, 2020, 14, 915-922.	1.4	9
46	A Novel GAA Hollow Cavity FinFET based biosensor for Cancer protein marker sensing. , 2020, , .		0
47	Impact of Graded Back-Barrier on Linearity of Recessed Gate InAlN/GaN HEMT. , 2020, , .		6
48	Gate Engineered GAA Silicon-Nanowire MOSFET for High Switching Performance. , 2020, , .		0
49	Impact of Metal Strip on Nanoscale Double Gate Overlap Tunnel FET. , 2020, , .		1
50	Prediction and forecast for COVID-19 Outbreak in India based on Enhanced Epidemiological Models. , 2020, , .		13
51	Temperature investigation of a Novel 3nm TF-Bulk FinFET for Improved Performance. , 2020, , .		7
52	Performance Analysis of a Novel Hetero-material InAs/GaAs Junctionless TFET. , 2020, , .		4
53	TCAD Analysis and Modelling of Gate-Stack Gate All Around Junctionless Silicon NWFET Based Bio-Sensor for Biomedical Application. , 2020, , .		2
54	The Effect of Gate Stack and High-Ä¸ Spacer on Device Performance of a Junctionless GAA FinFET. , 2020, , .		12

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55	Sub-10 nm High-k Dielectric SOI-FinFET for HighPerformance Low Power Applications. , 2020, , .		7
56	Rapid detection of biomolecules in a dielectric modulated GaN MOSHEMT. Journal of Materials Science: Materials in Electronics, 2020, 31, 16609-16615.	2.2	24
57	A Novel Trench FinFET as biosensor for early detection of dengue fever. , 2020, , .		0
58	Thermal Reliability of GaN-BTG-MOSFET for High-Performance Applications in Integrated Circuits. , 2020, , .		1
59	Microstates-based resting frontal alpha asymmetry approach for understanding affect and approach/withdrawal behavior. Scientific Reports, 2020, 10, 4228.	3.3	9
60	Increased efficiency of 23% for CIGS solar cell by using ITO as front contact. Materials Today: Proceedings, 2020, 28, 361-365.	1.8	17
61	Dielectric modulated transparent gate thin film transistor for biosensing applications. Materials Today: Proceedings, 2020, 28, 141-145.	1.8	12
62	Numerical analysis of Mg2Si/Si heterojunction DG-TFET for low power/high performance applications: Impact of non- idealities. Superlattices and Microstructures, 2020, 139, 106397.	3.1	26
63	Conducting Polymer Based Gas Sensor Using PNIN- Gate All Around - Tunnel FET. Silicon, 2020, 12, 2947-2955.	3.3	10
64	Investigation of electrical/analog performance and reliability of gate metal and source pocket engineered DG-TFET. Microsystem Technologies, 2020, , 1.	2.0	3
65	Built-in Reliability Investigation of Gate-Drain Underlapped PNIN-GAA-TFET for Improved Linearity and Reduced Intermodulation Distortion. Lecture Notes in Electrical Engineering, 2020, , 205-213.	0.4	1
66	Static and CV Analysis of Gate Engineered GAA Silicon Nanowire MOSFET for High-Performance Applications. Lecture Notes in Electrical Engineering, 2020, , 59-68.	0.4	0
67	Detection of Hazardous Analyte Using Transparent Gate Thin-Film Transistor. Lecture Notes in Networks and Systems, 2020, , 197-204.	0.7	1
68	Impact of metal silicide source electrode on polarity gate induced source in junctionless TFET. Applied Physics A: Materials Science and Processing, 2019, 125, 1.	2.3	20
69	TCAD analysis of transparent gate thin film transistor (TFT) for high performance applications. AIP Conference Proceedings, 2019, , .	0.4	0
70	Non-Quasi-Static Small-Signal Modeling of TGRC MOSFET in Parameter Perspective for RF/Microwave Applications. , 2019, , .		0
71	Effect of Temperature on GaAs Junctionless FinFET Using High-Î¹ Dielectric. , 2019, , .		1
72	Sub-30nm In2O5Sn gate electrode recessed channel MOSFET: A biosensor for early stage diagnostics. Vacuum, 2019, 164, 46-52.	3.5	19

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73	Toward the design of monolithic 23.1% efficient hysteresis and moisture free perovskite/c-Si HJ tandem solar cell: a numerical simulation study. Journal of Micromechanics and Microengineering, 2019, 29, 064001.	2.6	38
74	Numerical Simulations to Understand the Role of DIO Additive in PTB7:PC71BM Solar Cell. , 2019, , .		0
75	Carbon Nanotube Recessed Channel (CNT-RC) MOSFET for High Linearity/ULSI Applications. , 2019, , .		2
76	Low-Temperature Reliability of Sub-20nm 4H-SiC Trench MOSFET with Black Phosphorus Gate Material. , 2019, , .		1
77	Sub-20â€¯nm GaAs junctionless FinFET for biosensing application. Vacuum, 2019, 160, 467-471.	3.5	26
78	Analog and RF assessment of sub-20â€¯nm 4H-SiC trench gate MOSFET for high frequency applications. AEU - International Journal of Electronics and Communications, 2019, 98, 51-57.	2.9	8
79	RF noise modeling of Black Phosphorus Junctionless Trench MOSFET in strong inversion region. Superlattices and Microstructures, 2019, 125, 72-79.	3.1	8
80	Numerical simulations: Toward the design of 18.6% efficient and stable perovskite solar cell using reduced cerium oxide based ETL. Vacuum, 2019, 159, 173-181.	3.5	42
81	GaN Silicon-on-Insulator (SOI) N-Channel FinFET for High-Performance Low Power Applications. , 2019, , .		5
82	Comprehensive analysis of sub-20â€¯nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications. Superlattices and Microstructures, 2018, 116, 171-180.	3.1	34
83	Reliability Issues of In₂O₅Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. IEEE Transactions on Electron Devices, 2018, 65, 860-866.	3.0	47
84	Temperature Associated Reliability Issues of Heterogeneous Gate Dielectricâ€"Gate All Aroundâ€"Tunnel FET. IEEE Nanotechnology Magazine, 2018, 17, 41-48.	2.0	34
85	Temperature Reliability of Junctionless Twin Gate Recessed Channel (JL-TGRC) MOSFET with Different Gate Material for Low Power Digital-Logic Applications. , 2018, , .		0
86	Parametric Variation of ZnSe/TiO2Electron Transport Layer Based Perovskite Solar Cell: A Simulation Study and Optimization. , 2018, , .		2
87	Capacitive Analysis of Hetero Material Gate PNIN-DG-TFET Over Diverge Temperature Range for Superior RF/Microwave Performance. , 2018, , .		0
88	Electrical Characteristics Assessment of Gate Metal and Source Pocket Engineered DG-TFET for Low Power Analog Applications. , 2018, , .		3
89	Impact On Analog And Linearity Performance Of Nanoscale AlGaN/GaN HEMT With Variation In Surface Passivation Stack. Materials Today: Proceedings, 2018, 5, 17464-17471.	1.8	5
90	Gate Drain Underlapping: A Performance Enhancer For HD-GAA-TFET. Materials Today: Proceedings, 2018, 5, 17453-17463.	1.8	13

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91	Numerical Simulation of CeO_x ETL based Perovskite Solar Cell:- An Optimization Study for High Efficiency and Stability. , 2018, , .		3
92	Analysis of Varied Dielectrics as Surface Passivation on AlGaN/GaN HEMT for Analog Applications. , 2018, , .		4
93	GaAs Junctionless FinFET Using Si3N4 Spacer for High Performance Analog Application. , 2018, , .		4
94	A moisture stable, hysteresis-free semi-transparent perovskite solar cell with single wall carbon nanotubes. , 2018, , .		1
95	Performance Analysis of Heterojunction DMDG-TFET with Different Source Materials for Analog Application. , 2018, , .		3
96	Heterojunction DG-TFET-Analysis of Different Source Material for Improved Intermodulation. , 2018, , .		3
97	Source/Gate Material-Engineered Double Gate TFET for improved RF and linearity performance: a numerical simulation. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	34
98	Radiation Analysis of N-Channel TGRC-MOSFET: An X-Ray Dosimeter. IEEE Transactions on Electron Devices, 2018, 65, 5014-5020.	3.0	19
99	GaAs Junctionless FinFET Using High-k Dielectric for High-Performance Applications. , 2018, , .		3
100	Ultralow-power dielectric-modulated nanogap-embedded sub-20-nm TGRC-MOSFET for biosensing applications. Journal of Computational Electronics, 2018, 17, 1807-1815.	2.5	25
101	Linearity and Distortion Assessment of Black Phosphorus-Based Junctionless RC MOSFET. , 2018, , .		0
102	Investigation of Different Gate Materials for Improved Device Performance in RC MOSFET. , 2018, , .		1
103	Rear contact silicon solar cells with a-SiCX:H based front surface passivation for near-ultraviolet radiation stability. Superlattices and Microstructures, 2018, 122, 111-123.	3.1	6
104	In 2 O 5 Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications. AEU - International Journal of Electronics and Communications, 2018, 93, 233-241.	2.9	15
105	Influence of Fabrication Processes on Transport Properties of Superconducting Niobium Nitride Nanowires. Current Science, 2018, 114, 1443.	0.8	4
106	Cryogenic Measurement Set-Up for Characterization of Superconducting Nano Structures for Single-Photon Detection Applications. Current Science, 2018, 115, 1085.	0.8	4
107	Mathematical modeling insight of hetero gate dielectric-dual material gate-GAA-tunnel FET for VLSI/analog applications. Microsystem Technologies, 2017, 23, 4091-4098.	2.0	29
108	Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. Microsystem Technologies, 2017, 23, 4057-4064.	2.0	9

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109	Quantum analysis based extraction of frequency dependent intrinsic and extrinsic parameters for GEWE-SiNW MOSFET. Journal of Computational Electronics, 2017, 16, 61-73.	2.5	1
110	Effect of Nanoscale Structure on Reliability of Nano Devices and Sensors. , 2017, , 239-270.		1
111	Technology computer aided design of 29.5% efficient perovskite/interdigitated back contact silicon heterojunction mechanically stacked tandem solar cell for energy-efficient applications. Journal of Photonics for Energy, 2017, 7, 022503.	1.3	26
112	Numerical simulations of novel SiGe-based IBC-HJ solar cell for standalone and mechanically stacked tandem applications. Materials Research Bulletin, 2017, 93, 282-289.	5.2	22
113	Investigation of parasitic capacitances of In2O5Sn gate electrode recessed channel MOSFET for ULSI switching applications. Microsystem Technologies, 2017, 23, 5867-5874.	2.0	37
114	Numerical Simulation of N⁺ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature. IEEE Transactions on Electron Devices, 2017, 64, 1482-1488.	3.0	84
115	Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance. Superlattices and Microstructures, 2017, 102, 17-26.	3.1	63
116	Role of magnetic exchange interaction due to magnetic anisotropy on inverse spin Hall voltage at FeSi3%/Pt thin film bilayer interface. Journal of Magnetism and Magnetic Materials, 2017, 443, 159-164.	2.3	1
117	Performance investigation of heterogeneous gate dielectric-gate metal engineeredâ€“gate all around-tunnel FET for RF applications. Microsystem Technologies, 2017, 23, 4081-4090.	2.0	23
118	Gate metal engineered heterojunction DG-TFETs for superior analog performance and enhanced device reliability. , 2017, , .		6
119	Source material assessment of heterojunction DG-TFET for improved analog performance. , 2017, , .		4
120	Reliability of high-k gate stack on transparent gate recessed channel (TGRC) MOSFET. , 2017, , .		1
121	Influence of interface trap charge density on reliability issues of transparent gate recessed channel (TGRC) MOSFET. , 2017, , .		1
122	Twin gate rectangular recessed channel (TG-RRC) MOSFET for digital-logic applications. , 2017, , .		0
123	Small-signal modeling of In2O5Sn based transparent gate recessed channel MOSFET for microwave/RF applications. , 2017, , .		4
124	PNIN-GAA-tunnel FET with palladium catalytic metal gate as a highly sensitive hydrogen gas sensor. , 2017, , .		5
125	Influence of temperature variations on radio frequency performance of PNIN gate all around tunnel-FET. , 2017, , .		2
126	Interdigitated back contact silicon solar cell with perovskite layer for front surface passivation and ultraviolet radiation stability. , 2017, , .		0

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127	A Self - Consistently Coupled Drift Diffusion and Monte Carlo Simulator to Model Silicon Heterojunction Solar Cells. , 2017, , .		0
128	Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. Applied Physics A: Materials Science and Processing, 2016, 122, 1.	2.3	22
129	Rear contact SiGe solar cell with SiC passivated front surface for >90-percent external quantum efficiency and improved power conversion efficiency. Solar Energy, 2016, 135, 242-252.	6.1	20
130	Linearity performance of Gate Metal Engineered (GME) Omega Gate-Silicon Nanowire MOSFET: A TCAD study. , 2016, , .		3
131	Novel 4-terminal perovskite/SiC-based rear contact silicon tandem solar cell with 27.6 % PCE. , 2016, , .		4
132	Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability. IEEE Transactions on Device and Materials Reliability, 2016, 16, 227-234.	2.0	175
133	Numerical simulations: Toward the design of 27.6% efficient four-terminal semi-transparent perovskite/SiC passivated rear contact silicon tandem solar cell. Superlattices and Microstructures, 2016, 100, 656-666.	3.1	58
134	Numerical simulation of rear contact silicon solar cell with a novel front surface design for the suppression of interface recombination and improved absorption. Current Applied Physics, 2016, 16, 1581-1587.	2.4	23
135	Palladium Gate All Around - Hetero Dielectric -Tunnel FET based highly sensitive Hydrogen Gas Sensor. Superlattices and Microstructures, 2016, 100, 401-408.	3.1	27
136	Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. Microelectronics Reliability, 2016, 64, 235-241.	1.7	33
137	Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. Superlattices and Microstructures, 2016, 97, 630-641.	3.1	47
138	Temperature associated reliability issues of heterogeneous gate dielectric-gate all around-tunnel FET. , 2016, , .		8
139	Gate drain-overlapped-asymmetric gate dielectric-GAA-TFET: a solution for suppressed ambipolarity and enhanced ON state behavior. Applied Physics A: Materials Science and Processing, 2016, 122, 1.	2.3	44
140	Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. Superlattices and Microstructures, 2016, 91, 290-301.	3.1	32
141	TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET. Microelectronics Journal, 2016, 49, 36-42.	2.0	53
142	Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsystem Technologies, 2016, 22, 2665-2671.	2.0	41
143	Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. Microsystem Technologies, 2016, 22, 2655-2664.	2.0	10
144	Novel back-contact back-junction SiGe (BC-BJ SiGe) solar cell for improved power conversion efficiency. Microsystem Technologies, 2016, 22, 2673-2680.	2.0	18

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145	Front Surface Passivation Scheme for Back-Contact Back-Junction (BC-BJ) Silicon Solar Cell. Advanced Science Letters, 2016, 22, 815-820.	0.2	4
146	Novel SiC encapsulated coaxial silicon nanowire solar cell for optimal photovoltaic performance. , 2015, , .		3
147	Rear contact solar cell with ZrO2 nano structured front surface for efficient light trapping and enhanced surface passivation. , 2015, , .		3
148	Effect of dielectric engineering on analog and linearity performance of gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. , 2015, , .		4
149	Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. Journal of Computational Electronics, 2015, 14, 798-810.	2.5	39
150	Analytical drain current formulation for gate dielectric engineered dual material gate-gate all around-tunneling field effect transistor. Japanese Journal of Applied Physics, 2015, 54, 094202.	1.5	34
151	Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET. , 2014, , .		6
152	Impact of Channel Doping and Gate Length on Small Signal Behaviour of Gate Electrode Workfunction Engineered Silicon Nanowire MOSFET at THz Frequency. , 2014, , .		2
153	Novelautonomous surveillance system cum motion detector. , 2014, , .		0
154	Noise analysis of gate electrode work function engineered recessed channel (GEWE-RC) MOSFET. Journal of Physics: Conference Series, 2012, 367, 012013.	0.4	0
155	AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. Microelectronics Reliability, 2012, 52, 151-158.	1.7	28
156	Device linearity and intermodulation distortion comparison of dual material gate and conventional AlGaN/GaN high electron mobility transistor. Microelectronics Reliability, 2011, 51, 587-596.	1.7	76
157	Linearity-Distortion Analysis of GME-TRC MOSFET for High Performance and Wireless Applications. Journal of Semiconductor Technology and Science, 2011, 11, 169-181.	0.4	5
158	Hotâ€carrier reliability monitoring of DMG ISE SON MOSFET for improved analog performance. Microwave and Optical Technology Letters, 2010, 52, 770-775.	1.4	5
159	Design considerations and impact of technological parametric variations on RF/microwave performance of GEWEâ€RC MOSFET. Microwave and Optical Technology Letters, 2010, 52, 652-657.	1.4	1
160	Gate material engineeredâ€trapizoidal recessed channel MOSFET for highâ€performance analog and RF applications. Microwave and Optical Technology Letters, 2010, 52, 694-698.	1.4	2
161	Evaluation of multi-layered gate design on GME-TRC MOSFET for wireless applications. , 2010, , .		0
162	Two-dimensional threshold voltage model and design considerations for gate electrode work function engineered recessed channel nanoscale MOSFET: I. Semiconductor Science and Technology, 2009, 24, 065005.	2.0	4

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163	Investigation of multiâ€layeredâ€gate electrode workfunction engineered recessed channel (MLGEWEâ€RC) subâ€50â€‰nm MOSFET: A novel design. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2009, 22, 259-278.	1.9	6
164	Two dimensional simulation and analytical modeling of a novel ISE MOSFET with gate stack configuration. Microelectronic Engineering, 2009, 86, 2005-2014.	2.4	8
165	TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation. Superlattices and Microstructures, 2009, 46, 645-655.	3.1	20
166	Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGaN/GaN HEMT. Superlattices and Microstructures, 2008, 44, 37-53.	3.1	35
167	Laterally amalgamated DUal Material GAte Concave (L-DUMGAC) MOSFET for ULSI. Microelectronic Engineering, 2008, 85, 566-576.	2.4	25
168	Intermodulation distortion and linearity performance assessment of 50-nm gate length L-DUMGAC MOSFET for RFIC design. Superlattices and Microstructures, 2008, 44, 143-152.	3.1	27
169	Performance assessment and sub-threshold analysis of gate material engineered AlGaN/GaN HEMT for enhanced carrier transport efficiency. Microelectronics Journal, 2008, 39, 1416-1424.	2.0	6
170	TCAD Assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and Its Multilayered Gate Architecture—Part I: Hot-Carrier-Reliability Evaluation. IEEE Transactions on Electron Devices, 2008, 55, 2602-2613.	3.0	34
171	TCAD performance investigation of a novel MOSFET architecture of dual material gate insulated shallow extension silicon on nothing (DMG ISE SON) MOSFET for ULSI era. , 2008, , .		2
172	Impact of gate stack configuration onto the rf/analog performance of ISE MOSFET. , 2008, , .		0
173	Two dimensional analytical modeling of multi-layered dielectric G⁴ MOSFET-A novel design. , 2008, , .		0
174	RF performance investigation of DMG AlGaN/GaN high electron mobility transistor. , 2008, , .		0
175	GEWE-RC MOSFET: A solution to CMOS technology for RFIC design based on the concept of intercept point. , 2008, , .		1
176	DMG AlGaN/GaN HEMT: A solution to RF and wireless applications for reduced distortion performance. , 2008, , .		0
177	Gate Material Engineered-Trapizoidal Recessed Channel MOSFET (GME-TRC) for Ultra Large Scale Integration (ULSI). , 2008, , .		1
178	Two-dimensional analytical sub-threshold model of multi-layered gate dielectric recessed channel (MLaG-RC) nanoscale MOSFET. Semiconductor Science and Technology, 2008, 23, 045006.	2.0	5
179	On-state and RF performance investigation of sub-50 nm L-DUMGAC MOSFET design for high-speed logic and switching applications. Semiconductor Science and Technology, 2008, 23, 095009.	2.0	5
180	Exploring the effect on negative junction depth on electrical behaviour of sub-50nm GME-TRC MOSFET: A simulation study. , 2008, , .		0

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