

# Rishu Chaujar

## List of Publications by Year in descending order

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194  
papers

2,307  
citations

218677

26  
h-index

289244

40  
g-index

196  
all docs

196  
docs citations

196  
times ranked

725  
citing authors

#	ARTICLE	IF	CITATIONS
1	Interfacial Charge Analysis of Heterogeneous Gate Dielectric-Gate All Around-Tunnel FET for Improved Device Reliability. IEEE Transactions on Device and Materials Reliability, 2016, 16, 227-234.	2.0	175
2	Numerical Simulation of $N^+$ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature. IEEE Transactions on Electron Devices, 2017, 64, 1482-1488.	3.0	84
3	Device linearity and intermodulation distortion comparison of dual material gate and conventional AlGaIn/GaN high electron mobility transistor. Microelectronics Reliability, 2011, 51, 587-596.	1.7	76
4	Gate Drain Underlapped-PNIN-GAA-TFET for Comprehensively Upgraded Analog/RF Performance. Superlattices and Microstructures, 2017, 102, 17-26.	3.1	63
5	Numerical simulations: Toward the design of 27.6% efficient four-terminal semi-transparent perovskite/SiC passivated rear contact silicon tandem solar cell. Superlattices and Microstructures, 2016, 100, 656-666.	3.1	58
6	TCAD RF performance investigation of Transparent Gate Recessed Channel MOSFET. Microelectronics Journal, 2016, 49, 36-42.	2.0	53
7	Optimization of high-k and gate metal workfunction for improved analog and intermodulation performance of Gate Stack (GS)-GEWE-SiNW MOSFET. Superlattices and Microstructures, 2016, 97, 630-641.	3.1	47
8	Reliability Issues of $In_2O_5$ Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature. IEEE Transactions on Electron Devices, 2018, 65, 860-866.	3.0	47
9	Gate drain-overlapped-asymmetric gate dielectric-GAA-TFET: a solution for suppressed ambipolarity and enhanced ON state behavior. Applied Physics A: Materials Science and Processing, 2016, 122, 1.	2.3	44
10	Numerical simulations: Toward the design of 18.6% efficient and stable perovskite solar cell using reduced cerium oxide based ETL. Vacuum, 2019, 159, 173-181.	3.5	42
11	Analysis of novel transparent gate recessed channel (TGRC) MOSFET for improved analog behaviour. Microsystem Technologies, 2016, 22, 2665-2671.	2.0	41
12	Analog and RF Performance Evaluation of Junctionless Accumulation Mode (JAM) Gate Stack Gate All Around (GS-GAA) FinFET. Silicon, 2021, 13, 919-927.	3.3	41
13	Impact of device parameter variation on RF performance of gate electrode workfunction engineered (GEWE)-silicon nanowire (SiNW) MOSFET. Journal of Computational Electronics, 2015, 14, 798-810.	2.5	39
14	Toward the design of monolithic 23.1% efficient hysteresis and moisture free perovskite/c-Si HJ tandem solar cell: a numerical simulation study. Journal of Micromechanics and Microengineering, 2019, 29, 064001.	2.6	38
15	Investigation of parasitic capacitances of $In_2O_5$ Sn gate electrode recessed channel MOSFET for ULSI switching applications. Microsystem Technologies, 2017, 23, 5867-5874.	2.0	37
16	Analytical modeling and simulation of subthreshold behavior in nanoscale dual material gate AlGaIn/GaN HEMT. Superlattices and Microstructures, 2008, 44, 37-53.	3.1	35
17	TCAD Assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and Its Multilayered Gate Architecture; Part I: Hot-Carrier-Reliability Evaluation. IEEE Transactions on Electron Devices, 2008, 55, 2602-2613.	3.0	34
18	Analytical drain current formulation for gate dielectric engineered dual material gate-gate all around-tunneling field effect transistor. Japanese Journal of Applied Physics, 2015, 54, 094202.	1.5	34

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19	Comprehensive analysis of sub-20-nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications. Superlattices and Microstructures, 2018, 116, 171-180.	3.1	34
20	Temperature Associated Reliability Issues of Heterogeneous Gate Dielectric "Gate All Around" Tunnel FET. IEEE Nanotechnology Magazine, 2018, 17, 41-48.	2.0	34
21	Source/Gate Material-Engineered Double Gate TFET for improved RF and linearity performance: a numerical simulation. Applied Physics A: Materials Science and Processing, 2018, 124, 1.	2.3	34
22	Investigation of temperature variations on analog/RF and linearity performance of stacked gate GEWE-SiNW MOSFET for improved device reliability. Microelectronics Reliability, 2016, 64, 235-241.	1.7	33
23	Power gain assessment of ITO based Transparent Gate Recessed Channel (TGRC) MOSFET for RF/wireless applications. Superlattices and Microstructures, 2016, 91, 290-301.	3.1	32
24	TCAD Temperature Analysis of Gate Stack Gate All Around (GS-GAA) FinFET for Improved RF and Wireless Performance. Silicon, 2021, 13, 3741-3753.	3.3	32
25	Performance evaluation of linearity and intermodulation distortion of nanoscale GaN-SOI FinFET for RFIC design. AEU - International Journal of Electronics and Communications, 2020, 115, 153052.	2.9	31
26	Mathematical modeling insight of hetero gate dielectric-dual material gate-GAA-tunnel FET for VLSI/analog applications. Microsystem Technologies, 2017, 23, 4091-4098.	2.0	29
27	AC analysis of nanoscale GME-TRC MOSFET for microwave and RF applications. Microelectronics Reliability, 2012, 52, 151-158.	1.7	28
28	Intermodulation distortion and linearity performance assessment of 50-nm gate length L-DUMGAC MOSFET for RFIC design. Superlattices and Microstructures, 2008, 44, 143-152.	3.1	27
29	Palladium Gate All Around - Hetero Dielectric -Tunnel FET based highly sensitive Hydrogen Gas Sensor. Superlattices and Microstructures, 2016, 100, 401-408.	3.1	27
30	Technology computer aided design of 29.5% efficient perovskite/interdigitated back contact silicon heterojunction mechanically stacked tandem solar cell for energy-efficient applications. Journal of Photonics for Energy, 2017, 7, 022503.	1.3	26
31	Sub-20-nm GaAs junctionless FinFET for biosensing application. Vacuum, 2019, 160, 467-471.	3.5	26
32	Numerical analysis of Mg <sub>2</sub> Si/Si heterojunction DG-TFET for low power/high performance applications: Impact of non-idealities. Superlattices and Microstructures, 2020, 139, 106397.	3.1	26
33	Laterally amalgamated DUal Material Gate Concave (L-DUMGAC) MOSFET for ULSI. Microelectronic Engineering, 2008, 85, 566-576.	2.4	25
34	Ultralow-power dielectric-modulated nanogap-embedded sub-20-nm TGRC-MOSFET for biosensing applications. Journal of Computational Electronics, 2018, 17, 1807-1815.	2.5	25
35	Threshold voltage model for small geometry AlGaIn/GaN HEMTs based on analytical solution of 3-D Poisson's equation. Microelectronics Journal, 2007, 38, 1013-1020.	2.0	24
36	Rapid detection of biomolecules in a dielectric modulated GaN MOSHEMT. Journal of Materials Science: Materials in Electronics, 2020, 31, 16609-16615.	2.2	24

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37	Numerical simulation of rear contact silicon solar cell with a novel front surface design for the suppression of interface recombination and improved absorption. <i>Current Applied Physics</i> , 2016, 16, 1581-1587.	2.4	23
38	Performance investigation of heterogeneous gate dielectric-gate metal engineered "gate all around-tunnel FET for RF applications. <i>Microsystem Technologies</i> , 2017, 23, 4081-4090.	2.0	23
39	Influence of gate metal engineering on small-signal and noise behaviour of silicon nanowire MOSFET for low-noise amplifiers. <i>Applied Physics A: Materials Science and Processing</i> , 2016, 122, 1.	2.3	22
40	Numerical simulations of novel SiGe-based IBC-HJ solar cell for standalone and mechanically stacked tandem applications. <i>Materials Research Bulletin</i> , 2017, 93, 282-289.	5.2	22
41	TCAD assessment of Gate Electrode Workfunction Engineered Recessed Channel (GEWE-RC) MOSFET and its multi-layered gate architecture, Part II: Analog and large signal performance evaluation. <i>Superlattices and Microstructures</i> , 2009, 46, 645-655.	3.1	20
42	Rear contact SiGe solar cell with SiC passivated front surface for >90-percent external quantum efficiency and improved power conversion efficiency. <i>Solar Energy</i> , 2016, 135, 242-252.	6.1	20
43	Impact of metal silicide source electrode on polarity gate induced source in junctionless TFET. <i>Applied Physics A: Materials Science and Processing</i> , 2019, 125, 1.	2.3	20
44	Radiation Analysis of N-Channel TGRC-MOSFET: An X-Ray Dosimeter. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 5014-5020.	3.0	19
45	Sub-30nm In <sub>2</sub> O <sub>5</sub> Sn gate electrode recessed channel MOSFET: A biosensor for early stage diagnostics. <i>Vacuum</i> , 2019, 164, 46-52.	3.5	19
46	Novel back-contact back-junction SiGe (BC-BJ SiGe) solar cell for improved power conversion efficiency. <i>Microsystem Technologies</i> , 2016, 22, 2673-2680.	2.0	18
47	Increased efficiency of 23% for CIGS solar cell by using ITO as front contact. <i>Materials Today: Proceedings</i> , 2020, 28, 361-365.	1.8	17
48	Two-dimensional analytical model to characterize novel MOSFET architecture: insulated shallow extension MOSFET. <i>Semiconductor Science and Technology</i> , 2007, 22, 952-962.	2.0	16
49	Numerical Study of JAM-GS-GAA FinFET: A Fin Aspect Ratio Optimization for Upgraded Analog and Intermodulation Distortion Performance. <i>Silicon</i> , 2022, 14, 309-321.	3.3	16
50	In <sub>2</sub> O <sub>5</sub> Sn based transparent gate recessed channel MOSFET: RF small-signal model for microwave applications. <i>AEU - International Journal of Electronics and Communications</i> , 2018, 93, 233-241.	2.9	15
51	Effects of Neural Mechanisms of Pretask Resting EEG Alpha Information on Situational Awareness: A Functional Connectivity Approach. <i>Human Factors</i> , 2020, 62, 1150-1170.	3.5	14
52	Performance enhancement in a novel amalgamation of arsenide/antimonide tunneling interface with charge plasma junctionless-TFET. <i>AEU - International Journal of Electronics and Communications</i> , 2021, 133, 153669.	2.9	14
53	Hot-Carrier Reliability and Analog Performance Investigation of DMG-ISEGaS MOSFET. <i>IEEE Transactions on Electron Devices</i> , 2007, 54, 2556-2561.	3.0	13
54	Gate Drain Underlapping: A Performance Enhancer For HD-GAA-TFET. <i>Materials Today: Proceedings</i> , 2018, 5, 17453-17463.	1.8	13

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55	Prediction and forecast for COVID-19 Outbreak in India based on Enhanced Epidemiological Models. , 2020, , .		13
56	Analysis of structural parameters on sensitivity of black phosphorus junctionless recessed channel MOSFET for biosensing application. <i>Microsystem Technologies</i> , 2020, 26, 2227-2233.	2.0	12
57	The Effect of Gate Stack and High- $\kappa$ Spacer on Device Performance of a Junctionless GAA FinFET. , 2020, , .		12
58	Dielectric modulated transparent gate thin film transistor for biosensing applications. <i>Materials Today: Proceedings</i> , 2020, 28, 141-145.	1.8	12
59	Gate Oxide Variability Analysis of a Novel 3 nm Truncated Fin $\kappa$ FinFET for High Circuitry Performance. <i>Silicon</i> , 2021, 13, 3249-3256.	3.3	12
60	Design and Investigation of Recessed-T-Gate Double Channel HEMT with InGaN Back Barrier for Enhanced Performance. <i>Arabian Journal for Science and Engineering</i> , 2022, 47, 1109-1116.	3.0	12
61	Simulation of perovskite solar cell employing ZnO as electron transport layer (ETL) for improved efficiency. <i>Materials Today: Proceedings</i> , 2021, 46, 1684-1687.	1.8	11
62	Sensitivity Analysis of Biomolecule Nanocavity Immobilization in a Dielectric Modulated Triple-Hybrid Metal Gate-All-Around Junctionless NWFET Biosensor for Detecting Various Diseases. <i>Journal of Electronic Materials</i> , 2022, 51, 2236-2247.	2.2	11
63	Oxide bound impact on hot-carrier degradation for gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. <i>Microsystem Technologies</i> , 2016, 22, 2655-2664.	2.0	10
64	Conducting Polymer Based Gas Sensor Using PNIN- Gate All Around - Tunnel FET. <i>Silicon</i> , 2020, 12, 2947-2955.	3.3	10
65	TCAD investigation of ferroelectric based substrate MOSFET for digital application. <i>Silicon</i> , 2022, 14, 5075-5084.	3.3	10
66	Performance Investigation of 50-nm Insulated-Shallow-Extension Gate-Stack (ISEGaS) MOSFET for Mixed Mode Applications. <i>IEEE Transactions on Electron Devices</i> , 2007, 54, 365-368.	3.0	9
67	Effect of structured parameters on the hot-carrier immunity of transparent gate recessed channel (TGRC) MOSFET. <i>Microsystem Technologies</i> , 2017, 23, 4057-4064.	2.0	9
68	Numerical simulation and parametric assessment of GaN buffered trench gate MOSFET for low power applications. <i>IET Circuits, Devices and Systems</i> , 2020, 14, 915-922.	1.4	9
69	Microstates-based resting frontal alpha asymmetry approach for understanding affect and approach/withdrawal behavior. <i>Scientific Reports</i> , 2020, 10, 4228.	3.3	9
70	TCAD Analysis and Simulation of Double Metal Negative Capacitance FET (DM NCFET). , 2021, , .		9
71	Two dimensional simulation and analytical modeling of a novel ISE MOSFET with gate stack configuration. <i>Microelectronic Engineering</i> , 2009, 86, 2005-2014.	2.4	8
72	Temperature associated reliability issues of heterogeneous gate dielectric-gate all around-tunnel FET. , 2016, , .		8

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73	Analog and RF assessment of sub-20nm 4H-SiC trench gate MOSFET for high frequency applications. AEU - International Journal of Electronics and Communications, 2019, 98, 51-57.	2.9	8
74	RF noise modeling of Black Phosphorus Junctionless Trench MOSFET in strong inversion region. Superlattices and Microstructures, 2019, 125, 72-79.	3.1	8
75	Ultrascaled 10nm Trench gate mode InAlN / AlN HEMT with polarized doped buffer for high power microwave applications. International Journal of RF and Microwave Computer-Aided Engineering, 2022, 32, .	1.2	8
76	Analog/RF Performance and Effect of Temperature on Ferroelectric Layer Improved FET device with Spacer. Silicon, 2022, 14, 12269-12280.	3.3	8
77	Temperature investigation of a Novel 3nm TF-Bulk FinFET for Improved Performance. , 2020, , .		7
78	Sub-10 nm High-k Dielectric SOI-FinFET for HighPerformance Low Power Applications. , 2020, , .		7
79	Performance assessment and sub-threshold analysis of gate material engineered AlGaIn/GaN HEMT for enhanced carrier transport efficiency. Microelectronics Journal, 2008, 39, 1416-1424.	2.0	6
80	Investigation of multi-layered gate electrode workfunction engineered recessed channel (MLGEWE-RC) sub-50nm MOSFET: A novel design. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2009, 22, 259-278.	1.9	6
81	Implications of transport models on the analog performance of Gate Electrode Workfunction Engineered (GEWE) Silicon Nanowire MOSFET. , 2014, , .		6
82	Gate metal engineered heterojunction DG-TFETs for superior analog performance and enhanced device reliability. , 2017, , .		6
83	Rear contact silicon solar cells with a-SiC:H based front surface passivation for near-ultraviolet radiation stability. Superlattices and Microstructures, 2018, 122, 111-123.	3.1	6
84	Impact of Graded Back-Barrier on Linearity of Recessed Gate InAlN/GaN HEMT. , 2020, , .		6
85	Band gap and gate metal engineering of novel hetero-material InAs/GaAs-based JLTFET for improved wireless applications. Journal of Materials Science: Materials in Electronics, 2021, 32, 3155-3166.	2.2	6
86	Fin Aspect Ratio Optimization of Novel Junctionless Gate Stack Gate All Around (GS-GAA) FinFET for Analog/RF Applications. Lecture Notes in Electrical Engineering, 2021, , 59-67.	0.4	6
87	Numerical simulation of analog metrics and parasitic capacitances of GaAs GS-GAA FinFET for ULSI switching applications. European Physical Journal Plus, 2022, 137, 1.	2.6	6
88	A Numerical Study of Analog Parameter of Negative Capacitance Field Effect Transistor with Spacer. , 2021, , .		6
89	Detection of biomolecules in dielectric modulated double metal below ferroelectric layer FET with improved sensitivity. Journal of Materials Science: Materials in Electronics, 2022, 33, 13558-13567.	2.2	6
90	Two-dimensional analytical sub-threshold model of multi-layered gate dielectric recessed channel (MLaG-RC) nanoscale MOSFET. Semiconductor Science and Technology, 2008, 23, 045006.	2.0	5

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91	On-state and RF performance investigation of sub-50 nm L-DUMGAC MOSFET design for high-speed logic and switching applications. Semiconductor Science and Technology, 2008, 23, 095009.	2.0	5
92	Hot-carrier reliability monitoring of DMG ISE SON MOSFET for improved analog performance. Microwave and Optical Technology Letters, 2010, 52, 770-775.	1.4	5
93	PNIN-GAA-tunnel FET with palladium catalytic metal gate as a highly sensitive hydrogen gas sensor. , 2017, , .		5
94	Impact On Analog And Linearity Performance Of Nanoscale AlGaIn/GaN HEMT With Variation In Surface Passivation Stack. Materials Today: Proceedings, 2018, 5, 17464-17471.	1.8	5
95	Design Considerations and Capacitance Dependent Parametric Assessment of Gate Metal Engineered SiNW MOSFET for ULSI Switching Applications. Silicon, 2020, 12, 1501-1510.	3.3	5
96	Linearity-Distortion Analysis of GME-TRC MOSFET for High Performance and Wireless Applications. Journal of Semiconductor Technology and Science, 2011, 11, 169-181.	0.4	5
97	GaN Silicon-on-Insulator (SOI) N-Channel FinFET for High-Performance Low Power Applications. , 2019, , .		5
98	Analytical Modeling and Simulation of Potential and Electric Field Distribution in Dual Material Gate HEMT For Suppressed Short Channel Effects. , 2007, , .		4
99	Unified Subthreshold Model for Channel-Engineered Sub-100-nm Advanced MOSFET Structures. IEEE Transactions on Electron Devices, 2007, 54, 2475-2486.	3.0	4
100	Two-dimensional threshold voltage model and design considerations for gate electrode work function engineered recessed channel nanoscale MOSFET: I. Semiconductor Science and Technology, 2009, 24, 065005.	2.0	4
101	Effect of dielectric engineering on analog and linearity performance of gate electrode workfunction engineered (GEWE) silicon nanowire MOSFET. , 2015, , .		4
102	Novel 4-terminal perovskite/SiC-based rear contact silicon tandem solar cell with 27.6 % PCE. , 2016, , .		4
103	Source material assessment of heterojunction DG-TFET for improved analog performance. , 2017, , .		4
104	Small-signal modeling of In <sub>2</sub> O <sub>5</sub> Sn based transparent gate recessed channel MOSFET for microwave/RF applications. , 2017, , .		4
105	Analysis of Varied Dielectrics as Surface Passivation on AlGaIn/GaN HEMT for Analog Applications. , 2018, , .		4
106	GaAs Junctionless FinFET Using Si <sub>3</sub> N <sub>4</sub> Spacer for High Performance Analog Application. , 2018, , .		4
107	Performance Analysis of a Novel Hetero-material InAs/GaAs Junctionless TFET. , 2020, , .		4
108	Front Surface Passivation Scheme for Back-Contact Back-Junction (BC-BJ) Silicon Solar Cell. Advanced Science Letters, 2016, 22, 815-820.	0.2	4



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109	Influence of Fabrication Processes on Transport Properties of Superconducting Niobium Nitride Nanowires. Current Science, 2018, 114, 1443.	0.8	4
110	Cryogenic Measurement Set-Up for Characterization of Superconducting Nano Structures for Single-Photon Detection Applications. Current Science, 2018, 115, 1085.	0.8	4
111	Novel SiC encapsulated coaxial silicon nanowire solar cell for optimal photovoltaic performance. , 2015, , .		3
112	Rear contact solar cell with ZrO <sub>2</sub> nano structured front surface for efficient light trapping and enhanced surface passivation. , 2015, , .		3
113	Linearity performance of Gate Metal Engineered (GME) Omega Gate-Silicon Nanowire MOSFET: A TCAD study. , 2016, , .		3
114	Electrical Characteristics Assessment of Gate Metal and Source Pocket Engineered DG-TFET for Low Power Analog Applications. , 2018, , .		3
115	Numerical Simulation of CeO <sub>x</sub> ETL based Perovskite Solar Cell:- An Optimization Study for High Efficiency and Stability. , 2018, , .		3
116	Performance Analysis of Heterojunction DMDG-TFET with Different Source Materials for Analog Application. , 2018, , .		3
117	Heterojunction DG-TFET-Analysis of Different Source Material for Improved Intermodulation. , 2018, , .		3
118	GaAs Junctionless FinFET Using High-k Dielectric for High-Performance Applications. , 2018, , .		3
119	Investigation of electrical/analog performance and reliability of gate metal and source pocket engineered DG-TFET. Microsystem Technologies, 2020, , 1.	2.0	3
120	Reliability of Sub-20Ånm Black Phosphorus Trench (BP-T) MOSFET in High-Temperature Harsh Environment. Silicon, 2021, 13, 1277-1283.	3.3	3
121	RF, linearity and intermodulation distortion analysis with small-signal parameters extraction of tunable bandgap arsenide/antimonide tunneling interfaced JLTFET. Microsystem Technologies, 2022, 28, 2659-2667.	2.0	3
122	Impact of tunnel gate process variations on analog/radio frequency (microwave) and small signal parameters of hetero material tunneling interfaced charge plasma junctionless tunnel field effect transistor. International Journal of Circuit Theory and Applications, 2022, 50, 3626-3641.	2.0	3
123	Lateral channel engineered hetero material insulated shallow extension gate stack (HMISEGAS) MOSFET structure: high performance RF solution for MOS technology. Semiconductor Science and Technology, 2007, 22, 1097-1103.	2.0	2
124	3-dimensional analytical modeling and simulation of fully depleted AlGaIn/GaN modulation doped field effect transistor. , 2007, , .		2
125	Nanoscale insulated shallow extension MOSFET with Dual Material Gate for high performance analog operations. , 2007, , .		2
126	TCAD performance investigation of a novel MOSFET architecture of dual material gate insulated shallow extension silicon on nothing (DMG ISE SON) MOSFET for ULSI era. , 2008, , .		2



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127	Gate material engineered-Trapizoidal recessed channel MOSFET for high-performance analog and RF applications. Microwave and Optical Technology Letters, 2010, 52, 694-698.	1.4	2
128	Impact of Channel Doping and Gate Length on Small Signal Behaviour of Gate Electrode Workfunction Engineered Silicon Nanowire MOSFET at THz Frequency. , 2014, , .		2
129	Influence of temperature variations on radio frequency performance of PNIN gate all around tunnel-FET. , 2017, , .		2
130	Parametric Variation of ZnSe/TiO <sub>2</sub> Electron Transport Layer Based Perovskite Solar Cell: A Simulation Study and Optimization. , 2018, , .		2
131	Carbon Nanotube Recessed Channel (CNT-RC) MOSFET for High Linearity/ULSI Applications. , 2019, , .		2
132	TCAD Analysis and Modelling of Gate-Stack Gate All Around Junctionless Silicon NWFET Based Bio-Sensor for Biomedical Application. , 2020, , .		2
133	The Performance Analysis of 70nm T-gate InAlN/AlN MOS-HEMT using Graded Buffer. , 2021, , .		2
134	Influence of source electrode metal work function on polar gate prompted source hole plasma in arsenide/antimonide tunneling interfaced junctionless TFET. Journal of Micromechanics and Microengineering, 2022, 32, 044004.	2.6	2
135	Numerical investigation and temperature-based analysis of the analog performance of fully gate-covered junctionless FinFET. Computers and Electrical Engineering, 2022, 101, 108071.	4.8	2
136	Linearity Assessment in DMG ISEGaS MOSFET for RFIC Design. , 2007, , .		1
137	GEWE-RC MOSFET: A solution to CMOS technology for RFIC design based on the concept of intercept point. , 2008, , .		1
138	Gate Material Engineered-Trapizoidal Recessed Channel MOSFET (GME-TRC) for Ultra Large Scale Integration (ULSI). , 2008, , .		1
139	GEWE-RC MOSFET: High performance RF solution to CMOS technology. , 2008, , .		1
140	Design considerations and impact of technological parametric variations on RF/microwave performance of GEWE-RC MOSFET. Microwave and Optical Technology Letters, 2010, 52, 652-657.	1.4	1
141	Quantum analysis based extraction of frequency dependent intrinsic and extrinsic parameters for GEWE-SiNW MOSFET. Journal of Computational Electronics, 2017, 16, 61-73.	2.5	1
142	Effect of Nanoscale Structure on Reliability of Nano Devices and Sensors. , 2017, , 239-270.		1
143	Role of magnetic exchange interaction due to magnetic anisotropy on inverse spin Hall voltage at FeSi <sub>3</sub> /Pt thin film bilayer interface. Journal of Magnetism and Magnetic Materials, 2017, 443, 159-164.	2.3	1
144	Reliability of high-k gate stack on transparent gate recessed channel (TGRC) MOSFET. , 2017, , .		1

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145	Influence of interface trap charge density on reliability issues of transparent gate recessed channel (TGRC) MOSFET. , 2017, , .		1
146	A moisture stable, hysteresis-free semi-transparent perovskite solar cell with single wall carbon nanotubes. , 2018, , .		1
147	Investigation of Different Gate Materials for Improved Device Performance in RC MOSFET. , 2018, , .		1
148	Effect of Temperature on GaAs Junctionless FinFET Using High- $\epsilon$ Dielectric. , 2019, , .		1
149	Low-Temperature Reliability of Sub-20nm 4H-SiC Trench MOSFET with Black Phosphorus Gate Material. , 2019, , .		1
150	Impact of Metal Strip on Nanoscale Double Gate Overlap Tunnel FET. , 2020, , .		1
151	Thermal Reliability of GaN-BTG-MOSFET for High-Performance Applications in Integrated Circuits. , 2020, , .		1
152	Analysis of a Novel Nanoscale Vacuum Channel TF-FinFET. Silicon, 2021, 13, 3257-3269.	3.3	1
153	Investigation of TF-FinFET Based Biosensor for Early Diagnosis of Protein Carrying Diseases. , 2021, , .		1
154	Recessed Channel Carbon Nanotube Truncated Fin Finfet For High Performance ULSI Applications. , 2021, , .		1
155	Lower Fin Modulation Analysis for a Novel 5nm Top Bottom Gated Junctionless FinFET for improved performance. , 2021, , .		1
156	Investigation of a novel 5nm top bottom gated junctionless FinFET for improved switching and analog performance. Journal of Physics: Conference Series, 2021, 1921, 012100.	0.4	1
157	Technology Computer Aided Design of a Novel Fully Gate Covered Channel Junctionless SOI FinFET for high performance analog application. , 2021, , .		1
158	Built-in Reliability Investigation of Gate-Drain Underlapped PNIN-GAA-TFET for Improved Linearity and Reduced Intermodulation Distortion. Lecture Notes in Electrical Engineering, 2020, , 205-213.	0.4	1
159	Detection of Hazardous Analyte Using Transparent Gate Thin-Film Transistor. Lecture Notes in Networks and Systems, 2020, , 197-204.	0.7	1
160	Linearity Performance of Double Metal Negative Capacitance Field-Effect Transistors: A Numerical Study. , 2022, , .		1
161	Two-dimensional analytical sub-threshold modeling and simulation of Gate Material Engineered HEMT for enhanced carrier transport Efficiency. , 2007, , .		0
162	On-state and switching performance investigation of sub-50nm L-DUMGAC MOSFET design for high-speed logic applications. , 2007, , .		0

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163	Subthreshold performance consideration of a novel architecture: ISEGaS deca-nanometer MOSFET. , 2007, , .		0
164	Impact of gate stack configuration onto the rf/analog performance of ISE MOSFET. , 2008, , .		0
165	Two dimensional analytical modeling of multi-layered dielectric G<sup>4</sup> MOSFET-A novel design. , 2008, , .		0
166	RF performance investigation of DMG AlGa <sub>N</sub> /Ga <sub>N</sub> high electron mobility transistor. , 2008, , .		0
167	DMG AlGa <sub>N</sub> /Ga <sub>N</sub> HEMT: A solution to RF and wireless applications for reduced distortion performance. , 2008, , .		0
168	Exploring the effect on negative junction depth on electrical behaviour of sub-50nm GME-TRC MOSFET: A simulation study. , 2008, , .		0
169	Evaluation of multi-layered gate design on GME-TRC MOSFET for wireless applications. , 2010, , .		0
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