H-S Philip Wong

List of Publications by Year
in descending order

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412 papers	35,760 citations	5876 81 h-index	3997 176 g-index
417 all docs	417 docs citations	417 times ranked	22115 citing authors

#	Article	IF	Citations
1	Metalâ€“Oxide RRAM. Proceedings of the IEEE, 2012, 100, 1951-1970.	16.4	2,225
2	Phase Change Memory. Proceedings of the IEEE, 2010, 98, 2201-2227.	16.4	1,420
3	In-memory computing with resistive switching devices. Nature Electronics, 2018, 1, 333-343.	13.1	1,316
4	MoS ₂ transistors with 1-nanometer gate lengths. Science, 2016, 354, 99-102.	6.0	1,140
5	Nanoelectronic Programmable Synapses Based on Phase Change Materials for Brain-Inspired Computing. Nano Letters, 2012, 12, 2179-2186.	4.5	1,036
6	Synaptic electronics: materials, devices and applications. Nanotechnology, 2013, 24, 382001.	1.3	1,012
7	Graphene and two-dimensional materials for silicon technology. Nature, 2019, 573, 507-518.	13.7	936
8	Carbon nanotube computer. Nature, 2013, 501, 526-530.	13.7	903
9	Optoelectronic resistive random access memory for neuromorphic vision sensors. Nature Nanotechnology, 2019, 14, 776-782.	15.6	783
10	An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation. IEEE Transactions on Electron Devices, 2011, 58, 2729-2737.	1.6	731
11	A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Applicationâ€”Part I: Model of the Intrinsic Channel Region. IEEE Transactions on Electron Devices, 2007, 54, 3186-3194.	1.6	715
12	Face classification using electronic synapses. Nature Communications, 2017, 8, 15199.	5.8	683
13	Memory leads the way to better computing. Nature Nanotechnology, 2015, 10, 191-194.	15.6	671
14	A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Applicationâ€”Part II: Full Device Model and Circuit Performance Benchmarking. IEEE Transactions on Electron Devices, 2007, 54, 3195-3205.	1.6	587
15	Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature, 2017, 547, 74-78.	13.7	577
16	The End of Moore's Law: A New Beginning for Information Technology. Computing in Science and Engineering, 2017, 19, 41-50.	1.2	481
17	Artificial optic-neural synapse for colored and color-mixed pattern recognition. Nature Communications, 2018, 9, 5106.	5.8	462
18	Electronic synapses made of layered two-dimensional materials. Nature Electronics, 2018, 1, 458-465.	13.1	459

#	Article	IF	Citations
19	Recommended Methods to Study Resistive Switching Devices. Advanced Electronic Materials, 2019, 5, 1800143.	2.6	452
20	A Low Energy Oxideâ€Based Electronic Synaptic Device for Neuromorphic Visual Systems with Tolerance to Device Variation. Advanced Materials, 2013, 25, 1774-1779.	11.1	445
21	Continuous wireless pressure monitoring and mapping with ultra-small passive sensors for health monitoring and critical care. Nature Communications, 2014, 5, 5028.	5.8	418
22	Wafer-scale single-crystal hexagonal boron nitride monolayers on CuÂ(111). Nature, 2020, 579, 219-223.	13.7	409
23	The end of CMOS scaling. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2005, 21, 16-26.	0.8	361
24	Conduction mechanism of TiN/HfOx/Pt resistive switching memory: A trap-assisted-tunneling model. Applied Physics Letters, 2011, 99, .	1.5	327
25	HfO_x-Based Vertical Resistive Switching Random Access Memory Suitable for Bit-Cost-Effective Three-Dimensional Cross-Point Architecture. ACS Nano, 2013, 7, 2320-2325.	7.3	309
26	On the Switching Parameter Variation of Metal-Oxide RRAMâ€”Part I: Physical Modeling and Simulation Methodology. IEEE Transactions on Electron Devices, 2012, 59, 1172-1182.	1.6	300
27	Phase-Change Memoryâ€”Towards a Storage-Class Memory. IEEE Transactions on Electron Devices, 2017, 64, 4374-4385.	1.6	291
28	Generalized scale length for two-dimensional effects in MOSFETs. IEEE Electron Device Letters, 1998, 19, 385-387.	2.2	278
29	Extension and source/drain design for high-performance finFET devices. IEEE Transactions on Electron Devices, 2003, 50, 952-958.	1.6	266
30	Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory. Applied Physics Letters, 2011, 98, .	1.5	245
31	Cross-Point Memory Array Without Cell Selectorsâ€—Device Characteristics and Data Storage Pattern Dependencies. IEEE Transactions on Electron Devices, 2010, 57, 2531-2538.	1.6	241
32	How 2D semiconductors could extend Mooreâ€™s law. Nature, 2019, 567, 169-170.	13.7	222
33	A SPICE Compact Model of Metal Oxide Resistive Switching Memory With Variations. IEEE Electron Device Letters, 2012, 33, 1405-1407.	2.2	212
34	Technology and device scaling considerations for CMOS imagers. IEEE Transactions on Electron Devices, 1996, 43, 2131-2142.	1.6	211
35	Compact Modeling of Conducting-Bridge Random-Access Memory (CBRAM). IEEE Transactions on Electron Devices, 2011, 58, 1352-1360.	1.6	207
36	On the Switching Parameter Variation of Metal Oxide RRAMâ€”Part II: Model Corroboration and Device Design Strategy. IEEE Transactions on Electron Devices, 2012, 59, 1183-1188.	1.6	196

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37	Electrical tuning of phase-change antennas and metasurfaces. Nature Nanotechnology, 2021, 16, 667-672.	15.6	196
38	A 1 GHz Integrated Circuit with Carbon Nanotube Interconnects and Silicon Transistors. Nano Letters, 2008, 8, 706-709.	4.5	185
39	A Phenomenological Model for the Reset Mechanism of Metal Oxide RRAM. IEEE Electron Device Letters, 2010, 31, 1455-1457.	2.2	183
40	Brain-like associative learning using a nanoscale non-volatile phase change synaptic device array. Frontiers in Neuroscience, 2014, 8, 205.	1.4	176
41	Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes. IEEE Nanotechnology Magazine, 2009, 8, 498-504.	1.1	175
42	Ultra-Low-Energy Three-Dimensional Oxide-Based Electronic Synapses for Implementation of Robust High-Accuracy Neuromorphic Computation Systems. ACS Nano, 2014, 8, 6998-7004.	7.3	172
43	Self-aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel. , 0, , .		166
44	Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation. , 0, , .		165
45	Fermi level depinning in metal/Ge Schottky junction for metal source/drain Ge metal-oxide-semiconductor field-effect-transistor application. Journal of Applied Physics, 2009, 105, .	1.1	165
46	A Compact Model for Metalâ€“Oxide Resistive Random Access Memory With Experiment Verification. IEEE Transactions on Electron Devices, 2016, 63, 1884-1892.	1.6	163
47	Self-Aligned n-Channel Germanium MOSFETs With a Thin Ge Oxynitride Gate Dielectric and Tungsten Gate. IEEE Electron Device Letters, 2004, 25, 135-137.	2.2	161
48	CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes. Nano Letters, 2009, 9, 189-197.	4.5	161
49	Electrical characterization of germanium p-channel MOSFETs. IEEE Electron Device Letters, 2003, 24, 242-244.	2.2	160
50	Energy-Efficient Abundant-Data Computing: The N3XT 1,000x. Computer, 2015, 48, 24-33.	1.2	156
51	Statistical Study on the Schottky Barrier Reduction of Tunneling Contacts to CVD Synthesized MoS₂. Nano Letters, 2016, 16, 276-281.	4.5	156
52	Removable and Recyclable Conjugated Polymers for Highly Selective and High-Yield Dispersion and Release of Low-Cost Carbon Nanotubes. Journal of the American Chemical Society, 2016, 138, 802-805.	6.6	152
53	A neuromorphic visual system using RRAM synaptic devices with Sub-pJ energy and tolerance to variability: Experimental characterization and large-scale modeling. , 2012, , .		148
54	$hbox{Al}_{2}hbox{O}_{3}$-Based RRAM Using Atomic Layer Deposition (ALD) With 1-$muhbox{A}$ RESET Current. IEEE Electron Device Letters, 2010, 31, 1449-1451.	2.2	142

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55	Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. Nature Communications, 2019, 10, 2161.	5.8	141
56	On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, monte carlo simulation, and experimental characterization. , 2011, , .		138
57	Multi-level control of conductive nano-filament evolution in HfO₂ ReRAM by pulse-train operations. Nanoscale, 2014, 6, 5698-5702.	2.8	137
58	Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics. IEEE Transactions on Electron Devices, 2010, 57, 3137-3143.	1.6	127
59	Metal oxide-resistive memory using graphene-edge electrodes. Nature Communications, 2015, 6, 8407.	5.8	127
60	Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits. IEEE Nanotechnology Magazine, 2009, 8, 37-45.	1.1	125
61	Largeâ€Area Assembly of Densely Aligned Singleâ€Walled Carbon Nanotubes Using Solution Shearing and Their Application to Fieldâ€Effect Transistors. Advanced Materials, 2015, 27, 2656-2662.	11.1	123
62	Monitoring Oxygen Movement by Raman Spectroscopy of Resistive Random Access Memory with a Graphene-Inserted Electrode. Nano Letters, 2013, 13, 651-657.	4.5	121
63	Energy-Efficient Phase-Change Memory with Graphene as a Thermal Barrier. Nano Letters, 2015, 15, 6809-6814.	4.5	121
64	High-Performance p-Type Black Phosphorus Transistor with Scandium Contact. ACS Nano, 2016, 10, 4672-4677.	7.3	119
65	Variability in Carbon Nanotube Transistors: Improving Device-to-Device Consistency. ACS Nano, 2012, 6, 1109-1115.	7.3	115
66	Crystallization times of Geâ€“Te phase change materials as a function of composition. Applied Physics Letters, 2009, 95, .	1.5	114
67	Synthesis and size-dependent crystallization of colloidal germanium telluridenanoparticles. Journal of Materials Chemistry, 2010, 20, 1285-1291.	6.7	114
68	Cost-Effective, Transfer-Free, Flexible Resistive Random Access Memory Using Laser-Scribed Reduced Graphene Oxide Patterning Technology. Nano Letters, 2014, 14, 3214-3219.	4.5	114
69	SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors. Applied Physics Letters, 2001, 78, 1267-1269.	1.5	112
70	Thickness and stoichiometry dependence of the thermal conductivity of GeSbTe films. Applied Physics Letters, 2007, 91, .	1.5	112
71	Flexible Control of Block Copolymer Directed Selfâ€Assembly using Small, Topographical Templates: Potential Lithography Solution for Integrated Circuit Contact Hole Patterning. Advanced Materials, 2012, 24, 3107-3114.	11.1	112
72	Selective Synthesis and Device Applications of Semiconducting Single-Walled Carbon Nanotubes Using Isopropyl Alcohol as Feedstock. ACS Nano, 2012, 6, 7454-7462.	7.3	107

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73	Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET With Multiple Cylindrical Conducting Channels. IEEE Transactions on Electron Devices, 2007, 54, 2377-2385.	1.6	106
74	HfOx based vertical resistive random access memory for cost-effective 3D cross-point architecture without cell selector. , 2012, , .		106
75	Thermal Boundary Resistance Measurements for Phase-Change Memory Devices. IEEE Electron Device Letters, 2010, 31, 56-58.	2.2	105
76	Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs. , 2014, , .		105
77	Device and materials requirements for neuromorphic computing. Journal Physics D: Applied Physics, 2019, 52, 113001.	1.3	105
78	Carbon Nanotube Robust Digital VLSI. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 453-471.	1.9	104
79	Ultrafast Characterization of Phase-Change Material Crystallization Properties in the Melt-Quenched Amorphous Phase. Nano Letters, 2014, 14, 3419-3426.	4.5	102
80	Sensor-to-Digital Interface Built Entirely With Carbon Nanotube FETs. IEEE Journal of Solid-State Circuits, 2014, 49, 190-201.	3.5	101
81	High Current Density and Low Thermal Conductivity of Atomically Thin Semimetallic WTe₂. ACS Nano, 2016, 10, 7507-7514.	7.3	100
82	Impact of a Process Variation on Nanowire and Nanotube Device Performance. IEEE Transactions on Electron Devices, 2007, 54, 2369-2376.	1.6	98
83	Hyperdimensional computing with 3D VRRAM in-memory kernels: Device-architecture co-design for energy-efficient, error-resilient language recognition. , 2016, , .		95
84	Design Methods for Misaligned and Mispositioned Carbon-Nanotube Immune Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1725-1736.	1.9	93
85	Carbon Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfections. Digest of Technical Papers - IEEE International Solid-State Circuits Conference, 2007, , .	0.0	91
86	Distinctive in-Plane Cleavage Behaviors of Two-Dimensional Layered Materials. ACS Nano, 2016, 10, 8980-8988.	7.3	90
87	Carbon nanomaterials for non-volatile memories. Nature Reviews Materials, 2018, 3, .	23.3	87
88	Understanding Energy Efficiency Benefits of Carbon Nanotube Field-Effect Transistors for Digital VLSI. IEEE Nanotechnology Magazine, 2018, 17, 1259-1269.	1.1	87
89	Layered Semiconducting 2D Materials for Future Transistor Applications. Small Structures, 2021, 2, 2000103.	6.9	85
90	Brain-inspired computing exploiting carbon nanotube FETs and resistive RAM: Hyperdimensional computing case study. , 2018, , .		84

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91	A CMOS-integrated 'ISFET-operational amplifier' chemical sensor employing differential sensing. IEEE Transactions on Electron Devices, 1989, 36, 479-487.	1.6	83
92	Ternary content-addressable memory with MoS2 transistors for massively parallel data search. Nature Electronics, 2019, 2, 108-114.	13.1	83
93	Strained Si CMOS (SS CMOS) technology: opportunities and challenges. Solid-State Electronics, 2003, 47, 1133-1139.	0.8	82
94	VMR: VLSI-compatible metallic carbon nanotube removal for imperfection-immune cascaded multi-stage digital logic circuits using Carbon Nanotube FETs. , 2009, , .		82
95	TDI charge-coupled devices: Design and applications. IBM Journal of Research and Development, 1992, 36, 83-106.	3.2	81
96	Beyond the conventional transistor. Solid-State Electronics, 2005, 49, 755-762.	0.8	81
97	An Ultra-Low Reset Current Cross-Point Phase Change Memory With Carbon Nanotube Electrodes. IEEE Transactions on Electron Devices, 2012, 59, 1155-1163.	1.6	79
98	Real-Time Observation of the Electrode-Size-Dependent Evolution Dynamics of the Conducting Filaments in a SiO₂ Layer. ACS Nano, 2017, 11, 4097-4104.	7.3	79
99	Resistive random access memory (RRAM) technology: From material, device, selector, 3D integration to bottom-up fabrication. Journal of Electroceramics, 2017, 39, 21-38.	0.8	79
100	Nanoscale Bipolar and Complementary Resistive Switching Memory Based on Amorphous Carbon. IEEE Transactions on Electron Devices, 2011, 58, 3933-3939.	1.6	78
101	Ultralowâ€“switching current density multilevel phase-change memory on a flexible substrate. Science, 2021, 373, 1243-1247.	6.0	78
102	Low-Energy Robust Neuromorphic Computation Using Synaptic Devices. IEEE Transactions on Electron Devices, 2012, 59, 3489-3494.	1.6	76
103	Threshold Voltage and Onâ€“Off Ratio Tuning for Multiple-Tube Carbon Nanotube FETs. IEEE Nanotechnology Magazine, 2009, 8, 4-9.	1.1	75
104	Metal/III-V Schottky barrier height tuning for the design of nonalloyed III-V field-effect transistor source/drain contacts. Journal of Applied Physics, 2010, 107, .	1.1	75
105	A Circuit-Compatible SPICE model for Enhancement Mode Carbon Nanotube Field Effect Transistors. , 2006, , .		74
106	Analytical Modeling of the Suspended-Gate FET and Design Insights for Low-Power Logic. IEEE Transactions on Electron Devices, 2008, 55, 48-59.	1.6	71
107	The N3XT Approach to Energy-Efficient Abundant-Data Computing. Proceedings of the IEEE, 2019, 107, 19-48.	16.4	71
108	Discrete random dopant distribution effects in nanometer-scale MOSFETs. Microelectronics Reliability, 1998, 38, 1447-1456.	0.9	70

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109	Carbon Nanotube Circuit Integration up to Sub-20 nm Channel Lengths. ACS Nano, 2014, 8, 3434-3443.	7.3	70
110	Phonon and electron transport through Ge2Sb2Te5 films and interfaces bounded by metals. Applied Physics Letters, 2013, 102, .	1.5	68
111	Compact Model for Carbon Nanotube Field-Effect Transistors Including Nonidealities and Calibrated With Experimental Data Down to 9-nm Gate Length. IEEE Transactions on Electron Devices, 2013, 60, 1834-1843.	1.6	64
112	Two gates are better than one [double-gate MOSFET process]. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2003, 19, 48-62.	0.8	63
113	VLSI-Compatible Carbon Nanotube Doping Technique with Low Work-Function Metal Oxides. Nano Letters, 2014, 14, 1884-1890.	4.5	63
114	Efficient FPGAs using nanoelectromechanical relays. , 2010, , .		62
115	Hysteresis in Carbon Nanotube Transistors: Measurement and Analysis of Trap Density, Energy Level, and Spatial Distribution. ACS Nano, 2016, 10, 4599-4608.	7.3	62
116	Nanoscale phase change memory materials. Nanoscale, 2012, 4, 4382.	2.8	61
117	Resistive RAM-Centric Computing: Design and Modeling Methodology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2263-2273.	3.5	61
118	CMOS active pixel image sensors fabricated using a 1.8-V, 0.25-Î¼m CMOS technology. IEEE Transactions on Electron Devices, 1998, 45, 889-894.	1.6	60
119	A Monte Carlo study of the low resistance state retention of HfOx based resistive switching memory. Applied Physics Letters, 2012, 100, .	1.5	60
120	Schottky-Barrier Carbon Nanotube Field-Effect Transistor Modeling. IEEE Transactions on Electron Devices, 2007, 54, 439-445.	1.6	59
121	Picosecond Electric-Field-Induced Threshold Switching in Phase-Change Materials. Physical Review Letters, 2016, 117, 067601.	2.9	59
122	Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage. , 2009, , .		58
123	Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage. IEEE Transactions on Electron Devices, 2011, 58, 584-592.	1.6	58
124	Read/write schemes analysis for novel complementary resistive switches in passive crossbar memory arrays. Nanotechnology, 2010, 21, 465202.	1.3	57
125	The Effect of Donor/Acceptor Nature of Interface Traps on Ge MOSFET Characteristics. IEEE Transactions on Electron Devices, 2011, 58, 1015-1022.	1.6	57
126	Fast Spiking of a Mott VO₂â€“Carbon Nanotube Composite Device. Nano Letters, 2019, 19, 6751-6755.	4.5	56

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127	The Role of Ti Capping Layer in HfO_{<italic>x</italic>}-Based RRAM Devices. IEEE Electron Device Letters, 2014, 35, 912-914.	2.2	55
128	Analytical ballistic theory of carbon nanotube transistors: Experimental validation, device physics, parameter extraction, and performance projection. Journal of Applied Physics, 2008, 104, 124514.	1.1	54
129	Device study, chemical doping, and logic circuits based on transferred aligned single-walled carbon nanotubes. Applied Physics Letters, 2008, 93, .	1.5	54
130	Impact of fixed charge on metal-insulator-semiconductor barrier height reduction. Applied Physics Letters, 2011, 99, .	1.5	54
131	In Situ Tuning of Switching Window in a Gateâ€Controlled Bilayer Grapheneâ€Electrode Resistive Memory Device. Advanced Materials, 2015, 27, 7767-7774.	11.1	54
132	Fabrication of Metal Gated FinFETs Through Complete Gate Silicidation With Ni. IEEE Transactions on Electron Devices, 2004, 51, 2115-2120.	1.6	53
133	Optical Absorption Enhancement in Freestanding GaAs Thin Film Nanopyramid Arrays. Advanced Energy Materials, 2012, 2, 1254-1260.	10.2	52
134	Electron and hole mobility enhancement in strained SOI by wafer bonding. IEEE Transactions on Electron Devices, 2002, 49, 1566-1571.	1.6	51
135	Electronic and optical switching of solution-phase deposited SnSe2 phase change memory material. Journal of Applied Physics, 2011, 109, .	1.1	51
136	Nanometer-Scale ${m HfO}_{x}$ RRAM. IEEE Electron Device Letters, 2013, 34, 1005-1007.	2.2	51
137	Hysteresis-Free Carbon Nanotube Field-Effect Transistors. ACS Nano, 2017, 11, 4785-4791.	7.3	50
138	Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit. , 2011, , .		49
139	Hyperdimensional Computing Exploiting Carbon Nanotube FETs, Resistive RAM, and Their Monolithic 3D Integration. IEEE Journal of Solid-State Circuits, 2018, 53, 3183-3196.	3.5	49
140	Carbon nanotube correlation. , 2010, , .		48
141	In Situ Transmission Electron Microscopy Observation of Nanostructural Changes in Phase-Change Memory. ACS Nano, 2011, 5, 2742-2748.	7.3	48
142	Four-layer 3D vertical RRAM integrated with FinFET as a versatile computing unit for brain-inspired cognitive information processing. , 2016, , .		48
143	Experimental demonstration of high mobility Ge NMOS. , 2009, , .		47
144	Universal Selective Dispersion of Semiconducting Carbon Nanotubes from Commercial Sources Using a Supramolecular Polymer. ACS Nano, 2017, 11, 5660-5669.	7.3	47

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145	Frequency Response of Top-Gated Carbon Nanotube Field-Effect Transistors. IEEE Nanotechnology Magazine, 2004, 3, 383-387.	1.1	46
146	Analysis of Temperature in Phase Change Memory Scaling. IEEE Electron Device Letters, 2007, 28, 697-699.	2.2	46
147	Integrated wafer-scale growth and transfer of directional Carbon Nanotubes and misaligned-Carbon-Nanotube-immune logic structures. , 2008, , .		45
148	Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell. IEEE Transactions on Electron Devices, 2019, 66, 641-646.	1.6	43
149	Parasitic Capacitances: Analytical Models and Impact on Circuit-Level Performance. IEEE Transactions on Electron Devices, 2011, 58, 1361-1370.	1.6	42
150	Low-Temperature Side Contact to Carbon Nanotube Transistors: Resistance Distributions Down to 10 nm Contact Length. Nano Letters, 2019, 19, 1083-1089.	4.5	42
151	Characterization and Design of Logic Circuits in the Presence of Carbon Nanotube Density Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1103-1113.	1.9	41
152	A General Design Strategy for Block Copolymer Directed Self-Assembly Patterning of Integrated Circuits Contact Holes using an Alphabet Approach. Nano Letters, 2015, 15, 805-812.	4.5	41
153	Monolithic Integration of CMOS VLSI and Carbon Nanotubes for Hybrid Nanotechnology Applications. IEEE Nanotechnology Magazine, 2008, 7, 636-639.	1.1	40
154	Effect of annealing ambient and temperature on the electrical characteristics of atomic layer deposition Al2O3/In0.53Ga0.47As metal-oxide-semiconductor capacitors and MOSFETs. Journal of Applied Physics, 2012, 111, .	1.1	40
155	Unipolar n-Type Black Phosphorus Transistors with Low Work Function Contacts. Nano Letters, 2018, 18, 2822-2827.	4.5	40
156	Digital VLSI logic technology using Carbon Nanotube FETs. , 2009, , .		39
157	An Analytical Derivation of the Density of States, Effective Mass, and Carrier Density for Achiral Carbon Nanotubes. IEEE Transactions on Electron Devices, 2008, 55, 289-297.	1.6	38
158	Ultralow Voltage Crossbar Nonvolatile Memory Based on Energy-Reversible NEM Switches. IEEE Electron Device Letters, 2009, 30, 626-628.	2.2	38
159	Ultrafast terahertz-induced response of GeSbTe phase-change materials. Applied Physics Letters, 2014, 104, .	1.5	38
160	A non-iterative compact model for carbon nanotube FETs incorporating source exhaustion effects. , 2009, , .		37
161	Current Scaling in Aligned Carbon Nanotube Array Transistors With Local Bottom Gating. IEEE Electron Device Letters, 2010, 31, 644-646.	2.2	37
162	High-performance carbon nanotube field-effect transistors. , 2014, , .		37

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163	Low temperature (≤ 380°C) and high performance Ge CMOS technology with novel source/drain by metal-induced dopants activation and high-k/metal gate stack for monolithic 3D integration. , 2008, , .		36
164	ACCNTâ€"A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration. IEEE Transactions on Electron Devices, 2009, 56, 2969-2978.	1.6	36
165	Metal/III-V effective barrier height tuning using atomic layer deposition of high-Î¹/high-Î¹ bilayer interfaces. Applied Physics Letters, 2011, 99, 092107.	1.5	36
166	Design and optimization methodology for 3D RRAM arrays. , 2013, , .		36
167	Rapid Co-Optimization of Processing and Circuit Design to Overcome Carbon Nanotube Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1082-1095.	1.9	36
168	Engineering thermal and electrical interface properties of phase change memory with monolayer MoS2. Applied Physics Letters, 2019, 114, .	1.5	36
169	Characterization of the silicon on insulator film in bonded wafers by high resolution x-ray diffraction. Applied Physics Letters, 1999, 75, 787-789.	1.5	35
170	Phase change nanodot arrays fabricated using a self-assembly diblock copolymer approach. Applied Physics Letters, 2007, 91, 013104.	1.5	35
171	Experimental demonstration of array-level learning with phase change synaptic devices. , 2013, , .		35
172	Understanding the switching mechanism of interfacial phase change memory. Journal of Applied Physics, 2019, 125, .	1.1	35
173	Analysis of the Frequency Response of Carbon Nanotube Transistors. IEEE Nanotechnology Magazine, 2006, 5, 599-605.	1.1	34
174	1D Selection Device Using Carbon Nanotube FETs for High-Density Cross-Point Memory Arrays. IEEE Transactions on Electron Devices, 2015, 62, 2197-2204.	1.6	34
175	SAPIENS: A 64-kb RRAM-Based Non-Volatile Associative Memory for One-Shot Learning and Inference at the Edge. IEEE Transactions on Electron Devices, 2021, 68, 6637-6643.	1.6	34
176	A 3D Multi-Aperture Image Sensor Architecture. , 2006, , .		33
177	An Integrated Phase Change Memory Cell With Ge Nanowire Diode For Cross-Point Memory. , 2007, , .		33
178	Biomimetic Approaches for Fabricating High-Density Nanopatterned Arrays. Chemistry of Materials, 2007, 19, 839-843.	3.2	33
179	Combinational Logic Design Using Six-Terminal NEM Relays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 653-666.	1.9	32
180	AC conductance measurement and analysis of the conduction processes in HfOx based resistive switching memory. Applied Physics Letters, 2011, 99, .	1.5	31

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181	Block copolymer directed self-assembly (DSA) aware contact layer optimization for 10 nm 1D standard cell library. , 2013, , .		31
182	Vertical and Lateral Copper Transport through Graphene Layers. ACS Nano, 2015, 9, 8361-8367.	7.3	31
183	Spatial Separation of Carrier Spin by the Valley Hall Effect in Monolayer WSe₂ Transistors. Nano Letters, 2019, 19, 770-774.	4.5	31
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