Noriyuki Miura

List of Publications by Year in Descending Order

101 papers	795 citations	15 h-index	22 g-index
118 ext. papers	1,049 ext. citations	2.8 avg, IF	3.79 L-index

#	Paper	IF	Citations
101	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. *IEEE Transactions on Electron Devices*, **2021**, 68, 2077-2082	2.9	4
100	Diffusional Side-Channel Leakage From Unrolled Lightweight Block Ciphers: A Case Study of Power Analysis on PRINCE. *IEEE Transactions on Information Forensics and Security*, **2021**, 16, 1351-1364	8	0
99	Physical Attack Protection Techniques for IC Chip Level Hardware Security. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-10	2.6	2
98	Design and concept proof of an inductive impulse self-destructor in sense-and-react countermeasure against physical attacks. *Japanese Journal of Applied Physics*, **2021**, 60, SBBL01	1.4	5
97	Flush Code Eraser: Fast Attack Response Invalidating Cryptographic Sensitive Data. *IEEE Embedded Systems Letters*, **2020**, 12, 37-40	1	1
96	An IC-level countermeasure against laser fault injection attack by information leakage sensing based on laser-induced opto-electric bulk current density. *Japanese Journal of Applied Physics*, **2020** , 59, SGGL02	1.4	3
95	Side-Channel Leakage of Alarm Signal for a Bulk-Current-Based Laser Sensor. *Lecture Notes in Computer Science*, **2020**, 346-361	0.9	
94	. *IEEE Transactions on Computers*, **2020**, 69, 534-548	2.5	5
93	. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2747-2755	5.5	6
92	A Random Interrupt Dithering SAR Technique for Secure ADC Against Reference-Charge Side-Channel Attack. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 14-18	3.5	8
91	On-Chip Physical Attack Protection Circuits for Hardware Security : Invited Paper **2019**,		2
90	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2019**, 9, 502-510	1.7	6
89	Side-channel leakage from sensor-based countermeasures against fault injection attack. *Microelectronics Journal*, **2019**, 90, 63-71	1.8	3
88	Evaluation of Near-Field Undesired Radio Waves from Semiconductor Switching Circuits **2019**,		2
87	Evaluation of Undesired Radio Waves Below −170 dBm/Hz From Semiconductor Switching Devices for Impact on Wireless Communications. *IEEE Letters on EMC Practice and Applications*, **2019**, 1, 72-76	0.5	1
86	Magnetic Composite Sheets in IC Chip Packaging for Suppression of Undesired Noise Emission to Wireless Communication Channels **2019**,		2
85	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices **2019**,		1

84	A 0.72pJ/bit 400□2 Physical Random Number Generator Utilizing SAR Technique for Secure Implementation on Sensor Nodes. *IEICE Transactions on Electronics*, **2019**, E102.C, 530-537	0.4	
83	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs **2019**,		2
82	A Demonstration of a HT-Detection Method Based on Impedance Measurements of the Wiring Around ICs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1320-1324	3.5	7
81	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 2889-2897	5.5	6
80	A 286 F2/Cell Distributed Bulk-Current Sensor and Secure Flush Code Eraser Against Laser Fault Injection Attack on Cryptographic Processor. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 3174-3182	5.5	15
79	A 286F2/cell distributed bulk-current sensor and secure flush code eraser against laser fault injection attack **2018**,		7
78	Measurement and Analysis of Power Noise Characteristics for EMI Awareness of Power Delivery Networks in 3-D Through-Silicon Via Integration. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2018**, 8, 277-285	1.7	3
77	Design Methodology and Validity Verification for a Reactive Countermeasure Against EM Attacks. *Journal of Cryptology*, **2017**, 30, 373-391	2.1	10
76	An FPGA-compatible PLL-based sensor against fault injection attack **2017**,		4
75	Superior decoupling capacitor for three-dimensional LSI with ultrawide communication bus. *Japanese Journal of Applied Physics*, **2017**, 56, 04CC05	1.4	5
74	Protecting cryptographic integrated circuits with side-channel information. *IEICE Electronics Express* , **2017**, 14, 20162005-20162005	0.5	4
73	Exploiting Bitflip Detector for Non-invasive Probing and its Application to Ineffective Fault Analysis **2017**,		1
72	Enhancing reactive countermeasure against EM attacks with low overhead **2017**,		2
71	Chaos, deterministic non-periodic flow, for chip-package-board interactive PUF **2017**,		3
70	A 2.5ns-latency 0.39pJ/b 289□2/Gb/s ultra-light-weight PRINCE cryptographic processor **2017**,		1
69	A 500 MHz-BW -52.5 dB-THD Voltage-to-Time Converter Utilizing Two-Step Transition Inverter Delay Lines in 28 nm CMOS. *IEICE Transactions on Electronics*, **2017**, E100.C, 560-567	0.4	
68	A 500MHz-BW □2.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter **2016**,		3
67	Introduction to the Special Section on the 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC). *IEEE Journal of Solid-State Circuits*, **2016**, 51, 2207-2209	5.5	

66	Attack sensing against EM leakage and injection **2016**,		1
65	Ring Oscillator under Laser: Potential of PLL-based Countermeasure against Laser Fault Injection **2016**,		14
64	EMI performance of power delivery networks in 3D TSV integration **2016**,		4
63	On-chip substrate-bounce monitoring for laser-fault countermeasure **2016**,		5
62	PLL to the rescue **2016**,		18
61	Physical authentication using side-channel information **2016**,		4
60	EM attack sensor **2015**,		7
59	A 1 mm Pitch $80 times 80$ Channel 322 Hz Frame-Rate Multitouch Distribution Sensor With Two-Step Dual-Mode Capacitance Scan. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2741-2749	5.5	6
58	Proactive and reactive protection circuit techniques against EM leakage and injection **2015**,		1
57	Side-channel leakage on silicon substrate of CMOS cryptographic chip **2014**,		8
56	A local EM-analysis attack resistant cryptographic engine with fully-digital oscillator-based tamper-access sensor **2014**,		17
55	A 0.15-mm-Thick Noncontact Connector for MIPI Using a Vertical Directional Coupler. *IEEE Journal of Solid-State Circuits*, **2014**, 49, 223-231	5.5	7
54	A Scalable 3D Heterogeneous Multicore with an Inductive ThruChip Interface. *IEEE Micro*, **2014**, 1-1	1.8	
53	An intermittent-driven supply-current equalizer for 11x and 4x power-overhead savings in CPA-resistant 128bit AES cryptographic processor **2014**,		10
52	**2014**,		1
51	12.4 A 1mm-pitch 80×80-channel 322Hz-frame-rate touch sensor with two-step dual-mode capacitance scan **2014**,		4
50	Emulation of high-frequency substrate noise generation in CMOS digital circuits. *Japanese Journal of Applied Physics*, **2014**, 53, 04EE06	1.4	2
49	Integrated-circuit countermeasures against information leakage through EM radiation **2014**,		4

48	EM Attack Is Non-invasive? - Design Methodology and Validity Verification of EM Attack Sensor. *Lecture Notes in Computer Science*, **2014**, 1-16	0.9	16
47	Chip Level Simulation of Substrate Noise Coupling and Interference in RF ICs with CMOS Digital Noise Emulator. *IEICE Transactions on Electronics*, **2014**, E97.C, 546-556	0.4	1
46	Power Noise Measurements of Cryptographic VLSI Circuits Regarding Side-Channel Information Leakage. *IEICE Transactions on Electronics*, **2014**, E97.C, 272-279	0.4	3
45	Immunity evaluation of inverter chains against RF power on power delivery network **2013**,		2
44	A Scalable 3D Heterogeneous Multicore with an Inductive ThruChip Interface. *IEEE Micro*, **2013**, 33, 6-15	1.8	17
43	. *IEEE Journal of Solid-State Circuits*, **2013**, 48, 790-800	5.5	10
42	3D clock distribution using vertically/horizontally-coupled resonators **2013**,		6
41	**2013**,		1
40	A 0.15mm-thick non-contact connector for MIPI using vertical directional coupler **2013**,		8
39	. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2012**, 2, 249-256	5.2	14
38	Simultaneous 6-Gb/s Data and 10-mW Power Transmission Using Nested Clover Coils for Noncontact Memory Card. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2484-2495	5.5	3
37	A 7Gb/s/link non-contact memory module for multi-drop bus system using energy-equipartitioned coupled transmission line **2012**,		15
36	Progress of FD-SOI technology for monolithic pixel detectors **2012**,		9
35	A 65fJ/b Inter-Chip Inductive-Coupling Data Transceivers Using Charge-Recycling Technique for Low-Power Inter-Chip Communication in 3-D System Integration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1285-1294	2.6	9
34	A 12.5Gb/s/link non-contact multi drop bus system with impedance-matched transmission line couplers and Dicode partial-response channel transceivers **2012**,		4
33	A 0.025-0.45 W 60%-Efficiency Inductive-Coupling Power Transceiver With 5-Bit Dual-Frequency Feedforward Control for Non-Contact Memory Cards. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2496-2504	5.5	14
32	Rotary Coding for Power Reduction and S/N Improvement in Inductive-Coupling Data Communication. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 2643-2653	5.5	
31	Asynchronous Pulse Transmitter for Power Reduction in Inductive-Coupling Link. *Japanese Journal of Applied Physics*, **2012**, 51, 02BE06	1.4	2

30	Dynamic power control with a heterogeneous multi-core system using a 3-D wireless inductive coupling interconnect **2012**,		4
29	6W/25mm2 Wireless Power Transmission for Non-contact Wafer-Level Testing. *IEICE Transactions on Electronics*, **2012**, E95.C, 668-676	0.4	3
28	Asynchronous Pulse Transmitter for Power Reduction in Inductive-Coupling Link. *Japanese Journal of Applied Physics*, **2012**, 51, 02BE06	1.4	2
27	A 30 Gb/s/Link 2.2 Tb/s/mm ^{2} Inductively-Coupled Injection-Locking CDR for High-Speed DRAM Interface. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 2552-2559	5.5	14
26	. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 965-973	5.5	17
25	**2011**,		17
24	A 2Gb/s 1.8pJ/b/chip inductive-coupling through-chip bus for 128-Die NAND-Flash memory stacking **2010**,		15
23	2 Gb/s 15 pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking. *IEEE Journal of Solid-State Circuits*, **2010**, 45, 134-141	5.5	9
22	**2010**,		3
21	Simultaneous 6Gb/s data and 10mW power transmission using nested clover coils for non-contact memory card **2010**,		8
20	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 2269-2278	3.9	6
19	Inductive Coupled Communications. *Integrated Circuits and Systems*, **2010**, 79-125	0.2	4
18	47% power reduction and 91% area reduction in inductive-coupling programmable bus for NAND flash memory stacking **2009**,		6
17	A 2Gb/s 15pJ/b/chip Inductive-Coupling programmable bus for NAND Flash memory stacking **2009**,		16
16	A Wafer test method of inductive-coupling link **2009**,		6
15	An extended XY coil for noise reduction in inductive-coupling link **2009**,		7
14	A High-Speed Inductive-Coupling Link With Burst Transmission. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 947-955	5.5	45
13	A 0.14 pJ/b Inductive-Coupling Transceiver With Digitally-Controlled Precise Pulse Shaping. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 285-291	5.5	18

12	Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link. *Japanese Journal of Applied Physics*, **2008**, 47, 2749-2751	1.4	2
11	An 11Gb/s Inductive-Coupling Link with Burst Transmission **2008**,		35
10	A 2 Gb/s Bi-Directional Inter-Chip Data Transceiver With Differential Inductors for High Density Inductive Channel Array. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 2363-2369	5.5	6
9	A 1Tb/s 3W Inductive-Coupling Transceiver Chip **2007**,		9
8	60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique. *Japanese Journal of Applied Physics*, **2007**, 46, 2215-2219	1.4	9
7	A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping **2007**,		37
6	A 1 Tb/s 3 W Inductive-Coupling Transceiver for 3D-Stacked Inter-Chip Clock and Data Link. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 111-122	5.5	66
5	Crosstalk Countermeasures for High-Density Inductive-Coupling Channel Array. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 410-421	5.5	21
4	Wideband Inductive-coupling Interface for High-performance Portable System **2007**,		18
3	A 2Gb/s bi-directional inter-chip data transceiver with differential inductors for high density inductive channel array **2007**,		4
2	Measurement of Inductive Coupling in Wireless Superconnect. *Japanese Journal of Applied Physics*, **2006**, 45, 3286-3289	1.4	3
1	Perspective of Low-Power and High-Speed Wireless Inter-Chip Communications for SiP Integration **2006**,		6