## Noriyuki Miura

## List of Publications by Citations

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#	Paper	IF	Citations
101	A 1 Tb/s 3 W Inductive-Coupling Transceiver for 3D-Stacked Inter-Chip Clock and Data Link. <i>IEEE Journal of Solid-State Circuits</i> , <b>2007</b> , 42, 111-122	5.5	66
100	A High-Speed Inductive-Coupling Link With Burst Transmission. <i>IEEE Journal of Solid-State Circuits</i> , <b>2009</b> , 44, 947-955	5.5	45
99	A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping <b>2007</b> ,		37
98	An 11Gb/s Inductive-Coupling Link with Burst Transmission 2008,		35
97	Crosstalk Countermeasures for High-Density Inductive-Coupling Channel Array. <i>IEEE Journal of Solid-State Circuits</i> , <b>2007</b> , 42, 410-421	5.5	21
96	A 0.14 pJ/b Inductive-Coupling Transceiver With Digitally-Controlled Precise Pulse Shaping. <i>IEEE Journal of Solid-State Circuits</i> , <b>2008</b> , 43, 285-291	5.5	18
95	Wideband Inductive-coupling Interface for High-performance Portable System 2007,		18
94	PLL to the rescue <b>2016</b> ,		18
93	A local EM-analysis attack resistant cryptographic engine with fully-digital oscillator-based tamper-access sensor <b>2014</b> ,		17
92	A Scalable 3D Heterogeneous Multicore with an Inductive ThruChip Interface. <i>IEEE Micro</i> , <b>2013</b> , 33, 6-15	5 1.8	17
91	. IEEE Journal of Solid-State Circuits, <b>2011</b> , 46, 965-973	5.5	17
90	2011,		17
89	A 2Gb/s 15pJ/b/chip Inductive-Coupling programmable bus for NAND Flash memory stacking <b>2009</b> ,		16
88	EM Attack Is Non-invasive? - Design Methodology and Validity Verification of EM Attack Sensor. Lecture Notes in Computer Science, <b>2014</b> , 1-16	0.9	16
87	A 7Gb/s/link non-contact memory module for multi-drop bus system using energy-equipartitioned coupled transmission line <b>2012</b> ,		15
86	A 2Gb/s 1.8pJ/b/chip inductive-coupling through-chip bus for 128-Die NAND-Flash memory stacking <b>2010</b> ,		15
85	A 286 F2/Cell Distributed Bulk-Current Sensor and Secure Flush Code Eraser Against Laser Fault Injection Attack on Cryptographic Processor. <i>IEEE Journal of Solid-State Circuits</i> , <b>2018</b> , 53, 3174-3182	5.5	15

84	. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 249-256	5.2	14
83	A 0.025 <b>0</b> .45 W 60%-Efficiency Inductive-Coupling Power Transceiver With 5-Bit Dual-Frequency Feedforward Control for Non-Contact Memory Cards. <i>IEEE Journal of Solid-State Circuits</i> , <b>2012</b> , 47, 2496	5-2:504	14
82	A 30 Gb/s/Link 2.2 Tb/s/mm \$^{2}\$ Inductively-Coupled Injection-Locking CDR for High-Speed DRAM Interface. <i>IEEE Journal of Solid-State Circuits</i> , <b>2011</b> , 46, 2552-2559	5.5	14
81	Ring Oscillator under Laser: Potential of PLL-based Countermeasure against Laser Fault Injection <b>2016</b> ,		14
80	Design Methodology and Validity Verification for a Reactive Countermeasure Against EM Attacks. Journal of Cryptology, <b>2017</b> , 30, 373-391	2.1	10
79	. IEEE Journal of Solid-State Circuits, <b>2013</b> , 48, 790-800	5.5	10
78	An intermittent-driven supply-current equalizer for 11x and 4x power-overhead savings in CPA-resistant 128bit AES cryptographic processor <b>2014</b> ,		10
77	Progress of FD-SOI technology for monolithic pixel detectors <b>2012</b> ,		9
76	A 65fJ/b Inter-Chip Inductive-Coupling Data Transceivers Using Charge-Recycling Technique for Low-Power Inter-Chip Communication in 3-D System Integration. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2012</b> , 20, 1285-1294	2.6	9
75	2 Gb/s 15 pJ/b/chip Inductive-Coupling Programmable Bus for NAND Flash Memory Stacking. <i>IEEE Journal of Solid-State Circuits</i> , <b>2010</b> , 45, 134-141	5.5	9
74	A 1Tb/s 3W Inductive-Coupling Transceiver Chip <b>2007</b> ,		9
73	60% Power Reduction in Inductive-Coupling Inter-Chip Link by Current-Sensing Technique. <i>Japanese Journal of Applied Physics</i> , <b>2007</b> , 46, 2215-2219	1.4	9
72	Side-channel leakage on silicon substrate of CMOS cryptographic chip <b>2014</b> ,		8
71	A 0.15mm-thick non-contact connector for MIPI using vertical directional coupler <b>2013</b> ,		8
70	Simultaneous 6Gb/s data and 10mW power transmission using nested clover coils for non-contact memory card <b>2010</b> ,		8
69	A Random Interrupt Dithering SAR Technique for Secure ADC Against Reference-Charge Side-Channel Attack. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2020</b> , 67, 14-18	3.5	8
68	EM attack sensor <b>2015</b> ,		7
67	A Demonstration of a HT-Detection Method Based on Impedance Measurements of the Wiring Around ICs. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , <b>2018</b> , 65, 1320-1324	3.5	7

66	A 0.15-mm-Thick Noncontact Connector for MIPI Using a Vertical Directional Coupler. <i>IEEE Journal of Solid-State Circuits</i> , <b>2014</b> , 49, 223-231	5.5	7
65	An extended XY coil for noise reduction in inductive-coupling link 2009,		7
64	A 286F2/cell distributed bulk-current sensor and secure flush code eraser against laser fault injection attack <b>2018</b> ,		7
63	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , <b>2019</b> , 9, 502-510	1.7	6
62	A 1 mm Pitch \$80 times 80\$ Channel 322 Hz Frame-Rate Multitouch Distribution Sensor With Two-Step Dual-Mode Capacitance Scan. <i>IEEE Journal of Solid-State Circuits</i> , <b>2015</b> , 50, 2741-2749	5.5	6
61	. IEEE Journal of Solid-State Circuits, <b>2018</b> , 53, 2889-2897	5.5	6
60	3D clock distribution using vertically/horizontally-coupled resonators 2013,		6
59	. IEEE Transactions on Circuits and Systems I: Regular Papers, <b>2010</b> , 57, 2269-2278	3.9	6
58	47% power reduction and 91% area reduction in inductive-coupling programmable bus for NAND flash memory stacking <b>2009</b> ,		6
57	A Wafer test method of inductive-coupling link 2009,		6
56	A 2 Gb/s Bi-Directional Inter-Chip Data Transceiver With Differential Inductors for High Density Inductive Channel Array. <i>IEEE Journal of Solid-State Circuits</i> , <b>2008</b> , 43, 2363-2369	5.5	6
55	Perspective of Low-Power and High-Speed Wireless Inter-Chip Communications for SiP Integration <b>2006</b> ,		6
54	. IEEE Journal of Solid-State Circuits, <b>2020</b> , 55, 2747-2755	5.5	6
53	Superior decoupling capacitor for three-dimensional LSI with ultrawide communication bus. <i>Japanese Journal of Applied Physics</i> , <b>2017</b> , 56, 04CC05	1.4	5
52	. IEEE Transactions on Computers, <b>2020</b> , 69, 534-548	2.5	5
51	On-chip substrate-bounce monitoring for laser-fault countermeasure <b>2016</b> ,		5
50	Design and concept proof of an inductive impulse self-destructor in sense-and-react countermeasure against physical attacks. <i>Japanese Journal of Applied Physics</i> , <b>2021</b> , 60, SBBL01	1.4	5
49	An FPGA-compatible PLL-based sensor against fault injection attack <b>2017</b> ,		4

## (2006-2017)

48	Protecting cryptographic integrated circuits with side-channel information. <i>IEICE Electronics Express</i> , <b>2017</b> , 14, 20162005-20162005	0.5	4
47	12.4 A 1mm-pitch 80 <b>8</b> 0-channel 322Hz-frame-rate touch sensor with two-step dual-mode capacitance scan <b>2014</b> ,		4
46	Integrated-circuit countermeasures against information leakage through EM radiation 2014,		4
45	A 12.5Gb/s/link non-contact multi drop bus system with impedance-matched transmission line couplers and Dicode partial-response channel transceivers <b>2012</b> ,		4
44	Dynamic power control with a heterogeneous multi-core system using a 3-D wireless inductive coupling interconnect <b>2012</b> ,		4
43	A 2Gb/s bi-directional inter-chip data transceiver with differential inductors for high density inductive channel array <b>2007</b> ,		4
42	Inductive Coupled Communications. Integrated Circuits and Systems, 2010, 79-125	0.2	4
41	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. <i>IEEE Transactions on Electron Devices</i> , <b>2021</b> , 68, 2077-2082	2.9	4
40	EMI performance of power delivery networks in 3D TSV integration 2016,		4
39	Physical authentication using side-channel information <b>2016</b> ,		4
38	Side-channel leakage from sensor-based countermeasures against fault injection attack. <i>Microelectronics Journal</i> , <b>2019</b> , 90, 63-71	1.8	2
		1.0	3
37	An IC-level countermeasure against laser fault injection attack by information leakage sensing based on laser-induced opto-electric bulk current density. <i>Japanese Journal of Applied Physics</i> , <b>2020</b> , 59, SGGL02	1.4	3
37 36	based on laser-induced opto-electric bulk current density. Japanese Journal of Applied Physics, <b>2020</b>		
	based on laser-induced opto-electric bulk current density. <i>Japanese Journal of Applied Physics</i> , <b>2020</b> , 59, SGGL02  A 500MHz-BW B2.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter		3
36	based on laser-induced opto-electric bulk current density. <i>Japanese Journal of Applied Physics</i> , <b>2020</b> , 59, SGGL02  A 500MHz-BW \$\mathbb{B}\$2.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter <b>2016</b> ,		3
36 35	based on laser-induced opto-electric bulk current density. <i>Japanese Journal of Applied Physics</i> , <b>2020</b> , 59, SGGL02  A 500MHz-BW \$\mathbb{B}\$2.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter <b>2016</b> ,  Chaos, deterministic non-periodic flow, for chip-package-board interactive PUF <b>2017</b> ,  Simultaneous 6-Gb/s Data and 10-mW Power Transmission Using Nested Clover Coils for	1.4	3 3
36 35 34	based on laser-induced opto-electric bulk current density. <i>Japanese Journal of Applied Physics</i> , 2020, 59, SGGL02  A 500MHz-BW B2.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter 2016,  Chaos, deterministic non-periodic flow, for chip-package-board interactive PUF 2017,  Simultaneous 6-Gb/s Data and 10-mW Power Transmission Using Nested Clover Coils for Noncontact Memory Card. <i>IEEE Journal of Solid-State Circuits</i> , 2012, 47, 2484-2495	1.4	3 3 3

30	Power Noise Measurements of Cryptographic VLSI Circuits Regarding Side-Channel Information Leakage. <i>IEICE Transactions on Electronics</i> , <b>2014</b> , E97.C, 272-279	0.4	3
29	Measurement and Analysis of Power Noise Characteristics for EMI Awareness of Power Delivery Networks in 3-D Through-Silicon Via Integration. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , <b>2018</b> , 8, 277-285	1.7	3
28	On-Chip Physical Attack Protection Circuits for Hardware Security : Invited Paper 2019,		2
27	Evaluation of Near-Field Undesired Radio Waves from Semiconductor Switching Circuits 2019,		2
26	Immunity evaluation of inverter chains against RF power on power delivery network 2013,		2
25	Enhancing reactive countermeasure against EM attacks with low overhead 2017,		2
24	Emulation of high-frequency substrate noise generation in CMOS digital circuits. <i>Japanese Journal of Applied Physics</i> , <b>2014</b> , 53, 04EE06	1.4	2
23	Asynchronous Pulse Transmitter for Power Reduction in Inductive-Coupling Link. <i>Japanese Journal of Applied Physics</i> , <b>2012</b> , 51, 02BE06	1.4	2
22	Capacitor-Shunted Transmitter for Power Reduction in Inductive-Coupling Clock Link. <i>Japanese Journal of Applied Physics</i> , <b>2008</b> , 47, 2749-2751	1.4	2
21	Asynchronous Pulse Transmitter for Power Reduction in Inductive-Coupling Link. <i>Japanese Journal of Applied Physics</i> , <b>2012</b> , 51, 02BE06	1.4	2
20	Magnetic Composite Sheets in IC Chip Packaging for Suppression of Undesired Noise Emission to Wireless Communication Channels <b>2019</b> ,		2
19	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs <b>2019</b> ,		2
18	Physical Attack Protection Techniques for IC Chip Level Hardware Security. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , <b>2021</b> , 1-10	2.6	2
17	Flush Code Eraser: Fast Attack Response Invalidating Cryptographic Sensitive Data. <i>IEEE Embedded Systems Letters</i> , <b>2020</b> , 12, 37-40	1	1
16	Exploiting Bitflip Detector for Non-invasive Probing and its Application to Ineffective Fault Analysis <b>2017</b> ,		1
15	A 2.5ns-latency 0.39pJ/b 289fh2/Gb/s ultra-light-weight PRINCE cryptographic processor <b>2017</b> ,		1
14	Proactive and reactive protection circuit techniques against EM leakage and injection 2015,		1
13	2014,		1

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12	2013,		1
11	Evaluation of Undesired Radio Waves Below 1170 dBm/Hz From Semiconductor Switching Devices for Impact on Wireless Communications. <i>IEEE Letters on EMC Practice and Applications</i> , <b>2019</b> , 1, 72-76	0.5	1
10	Chip Level Simulation of Substrate Noise Coupling and Interference in RF ICs with CMOS Digital Noise Emulator. <i>IEICE Transactions on Electronics</i> , <b>2014</b> , E97.C, 546-556	0.4	1
9	Attack sensing against EM leakage and injection <b>2016</b> ,		1
8	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices <b>2019</b> ,		1
7	Diffusional Side-Channel Leakage From Unrolled Lightweight Block Ciphers: A Case Study of Power Analysis on PRINCE. <i>IEEE Transactions on Information Forensics and Security</i> , <b>2021</b> , 16, 1351-1364	8	O
6	Introduction to the Special Section on the 2015 IEEE Asian Solid-State Circuits Conference (A-SSCC). <i>IEEE Journal of Solid-State Circuits</i> , <b>2016</b> , 51, 2207-2209	5.5	
5	A 500 MHz-BW -52.5 dB-THD Voltage-to-Time Converter Utilizing Two-Step Transition Inverter Delay Lines in 28 nm CMOS. <i>IEICE Transactions on Electronics</i> , <b>2017</b> , E100.C, 560-567	0.4	
4	A Scalable 3D Heterogeneous Multicore with an Inductive ThruChip Interface. <i>IEEE Micro</i> , <b>2014</b> , 1-1	1.8	
3	Rotary Coding for Power Reduction and S/N Improvement in Inductive-Coupling Data Communication. <i>IEEE Journal of Solid-State Circuits</i> , <b>2012</b> , 47, 2643-2653	5.5	
2	Side-Channel Leakage of Alarm Signal for a Bulk-Current-Based Laser Sensor. <i>Lecture Notes in Computer Science</i> , <b>2020</b> , 346-361	0.9	
1	A 0.72pJ/bit 400fh2 Physical Random Number Generator Utilizing SAR Technique for Secure Implementation on Sensor Nodes. <i>IEICE Transactions on Electronics</i> , <b>2019</b> , E102.C, 530-537	0.4	