Nuo Xu

List of Publications by Year
in descending order

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45	783	623734	552781
papers	citations	14 h-index	26 g-index

46	46	46	1135
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Complementary Memtransistor-Based Multilayer Neural Networks for Online Supervised Learning Through (Anti-)Spike-Timing-Dependent Plasticity. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 6640-6651.	11.3	4
2	Implementation of Highly Reliable and Energyâ€Efficient Nonvolatile Inâ€Memory Computing using Multistate Domain Wall Spinâ€“Orbit Torque Device. Advanced Intelligent Systems, 2022, 4, .	6.1	13
3	Reconfigurable Physical Unclonable Function Based on Spin-Orbit Torque Induced Chiral Domain Wall Motion. IEEE Electron Device Letters, 2021, 42, 597-600.	3.9	8
4	Nano-scaled transistor reliability characterization at nano-second regime. Science China Information Sciences, 2021, 64, 1.	4.3	1
5	A Dual Magnetic Tunnel Junctionâ€Based Neuromorphic Device. Advanced Intelligent Systems, 2020, 2, 2000143.	6.1	11
6	Thermally Assisted Skyrmion Memory (TA-SKM). IEEE Electron Device Letters, 2020, 41, 932-935.	3.9	3
7	Piezoelectric Tunnel FET With a Steep Slope. IEEE Electron Device Letters, 2020, 41, 948-951.	3.9	2
8	Experimental Validation of Depolarization Field Produced Voltage Gains in Negative Capacitance Field-Effect Transistors. IEEE Transactions on Electron Devices, 2019, 66, 4419-4424.	3.0	26
9	ZrO₂ Ferroelectric FET for Non-volatile Memory Application. IEEE Electron Device Letters, 2019, 40, 1419-1422.	3.9	38
10	An Eulerâ€“Lagrange Equation Oriented Solution for Write Energy Minimization of STT-MRAM. IEEE Transactions on Electron Devices, 2019, 66, 3686-3689.	3.0	5
11	Nanocrystal-Embedded-Insulator (NEI) Ferroelectric Field-Effect Transistor Featuring Low Operating Voltages and Improved Synaptic Behavior. IEEE Electron Device Letters, 2019, 40, 1933-1936.	3.9	20
12	Exploring the Designs of p-Type Piezoelectric FinFETs Based on NEGF Transport Simulations Comprising Phonon Scattering. IEEE Transactions on Electron Devices, 2019, 66, 4982-4988.	3.0	2
13	A Spinâ€“Orbitâ€Torque Memristive Device. Advanced Electronic Materials, 2019, 5, 1800782.	5.1	51
14	Optimal Tuning of Memristor Conductance Variation in Spiking Neural Networks for Online Unsupervised Learning. IEEE Transactions on Electron Devices, 2019, 66, 2844-2849.	3.0	14
15	Memristors: A Spinâ€“Orbitâ€Torque Memristive Device (Adv. Electron. Mater. 4/2019). Advanced Electronic Materials, 2019, 5, 1970022.	5.1	4
16	Voltage-Controlled Skyrmion Memristor for Energy-Efficient Synapse Applications. IEEE Electron Device Letters, 2019, 40, 635-638.	3.9	31
17	Complementary Graphene-Ferroelectric Transistors (C-GFTs) as Synapses with Modulatable Plasticity for Supervised Learning. , 2019, , .		6
18	Alleviating Conductance Nonlinearity via Pulse Shape Designs in TaO_{<italic>x</italic>} Memristive Synapses. IEEE Transactions on Electron Devices, 2019, 66, 810-813.	3.0	17

#	Article	IF	Citations
19	Incomplete Dipoles Flipping Produced Near Hysteresis-Free Negative Capacitance Transistors. IEEE Electron Device Letters, 2019, 40, 329-332.	3.9	30
20	Reconfigurable Skyrmion Logic Gates. Nano Letters, 2018, 18, 1180-1184.	9.1	201
21	Binary and Ternary True Random Number Generators Based on Spin Orbit Torque. , 2018, , .		13
22	Ultra-Low Power Nano-electromechanical Switch Realized by Controlled and Reversible Crack. , 2018, , .		0
23	Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs with Sub-kT/q Swing. IEEE Electron Device Letters, 2018, , 1-1.	3.9	14
24	Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions. IEEE Transactions on Electron Devices, 2018, 65, 4687-4693.	3.0	8
25	Effect of measurement speed (Î¼s-800 ps) on the characterization of reliability behaviors for FDSOI nMOSFETs. , 2018, , .		3
26	Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. IEEE Electron Device Letters, 2015, 36, 862-864.	3.9	15
27	Comprehensive understanding of hot carrier degradation in multiple-fin SOI FinFETs. , 2015, , .		7
28	Oxygen-inserted SegFET: A candidate for 10-nm node system-on-chip applications. , 2014, , .		0
29	Enhancement of band-to-band tunneling in mono-layer transition metal dichalcogenides two-dimensional materials by vacancy defects. Applied Physics Letters, 2014, 104, .	3.3	34
30	NEM relay design for compact, ultra-low-power digital logic circuits. , 2014, , .		7
31	Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications. , 2014, , .		36
32	Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. IEEE Transactions on Electron Devices, 2014, 61, 3345-3349.	3.0	11
33	Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. IEEE Transactions on Electron Devices, 2014, 61, 3296-3302.	3.0	11
34	Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. IEEE Transactions on Electron Devices, 2013, 60, 1790-1793.	3.0	15
35	Fabrication of $hbox{Si}_{1 - x}hbox{Ge}_{x}/hbox{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{m ON}$ and Reduced Layout-Width Dependence. IEEE Transactions on Electron Devices, 2013, 60, 153-158.	3.0	6
36	Variation-aware study of BJT-based capacitorless DRAM cell scaling limit. , 2012, , .		0

#	Article	IF	Citations
37	Effectiveness of strained-Si technology for thin-body MOSFETs. , 2012, , .		1
38	Impact of back biasing on carrier transport in ultra-thin-body and BOX (UTBB) Fully Depleted SOI MOSFETs. , 2012, , .		19
39	Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. IEEE Electron Device Letters, 2012, 33, 318-320.	3.9	24
40	Effectiveness of Stressors in Aggressively Scaled FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 1592-1598.	3.0	39
41	First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. IEEE Transactions on Electron Devices, 2012, 59, 2273-2276.	3.0	7
42	Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. IEEE Transactions on Device and Materials Reliability, 2011, 11, 378-386.	2.0	12
43	Study of High-Performance Ge pMOSFET Scaling Accounting for Direct Source-to-Drain Tunneling. IEEE Transactions on Electron Devices, 2011, 58, 2895-2902.	3.0	6
44	MuGFET carrier mobility and velocity: Impacts of fin aspect ratio, orientation and stress. , 2010, , .		7
45	Predictive Compact Modeling for Strain Effects in Nanoscale Transistors. , 2009, , .		1