

# Nuo Xu

## List of Publications by Year in descending order

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g-index

46  
all docs

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docs citations

46  
times ranked

1135  
citing authors

#	ARTICLE	IF	CITATIONS
1	Reconfigurable Skyrmion Logic Gates. Nano Letters, 2018, 18, 1180-1184.	9.1	201
2	A Spin-Orbit Torque Memristive Device. Advanced Electronic Materials, 2019, 5, 1800782.	5.1	51
3	Effectiveness of Stressors in Aggressively Scaled FinFETs. IEEE Transactions on Electron Devices, 2012, 59, 1592-1598.	3.0	39
4	ZrO <sub>2</sub> Ferroelectric FET for Non-volatile Memory Application. IEEE Electron Device Letters, 2019, 40, 1419-1422.	3.9	38
5	Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications. , 2014, , .		36
6	Enhancement of band-to-band tunneling in mono-layer transition metal dichalcogenides two-dimensional materials by vacancy defects. Applied Physics Letters, 2014, 104, .	3.3	34
7	Voltage-Controlled Skyrmion Memristor for Energy-Efficient Synapse Applications. IEEE Electron Device Letters, 2019, 40, 635-638.	3.9	31
8	Incomplete Dipoles Flipping Produced Near Hysteresis-Free Negative Capacitance Transistors. IEEE Electron Device Letters, 2019, 40, 329-332.	3.9	30
9	Experimental Validation of Depolarization Field Produced Voltage Gains in Negative Capacitance Field-Effect Transistors. IEEE Transactions on Electron Devices, 2019, 66, 4419-4424.	3.0	26
10	Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. IEEE Electron Device Letters, 2012, 33, 318-320.	3.9	24
11	Nanocrystal-Embedded-Insulator (NEI) Ferroelectric Field-Effect Transistor Featuring Low Operating Voltages and Improved Synaptic Behavior. IEEE Electron Device Letters, 2019, 40, 1933-1936.	3.9	20
12	Impact of back biasing on carrier transport in ultra-thin-body and BOX (UTBB) Fully Depleted SOI MOSFETs. , 2012, , .		19
13	Alleviating Conductance Nonlinearity via Pulse Shape Designs in TaO <sub>x</sub> Memristive Synapses. IEEE Transactions on Electron Devices, 2019, 66, 810-813.	3.0	17
14	Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. IEEE Transactions on Electron Devices, 2013, 60, 1790-1793.	3.0	15
15	Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. IEEE Electron Device Letters, 2015, 36, 862-864.	3.9	15
16	Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs with Sub-kT/q Swing. IEEE Electron Device Letters, 2018, , 1-1.	3.9	14
17	Optimal Tuning of Memristor Conductance Variation in Spiking Neural Networks for Online Unsupervised Learning. IEEE Transactions on Electron Devices, 2019, 66, 2844-2849.	3.0	14
18	Binary and Ternary True Random Number Generators Based on Spin Orbit Torque. , 2018, , .		13

#	ARTICLE	IF	CITATIONS
19	Implementation of Highly Reliable and Energy-Efficient Nonvolatile In-Memory Computing using Multistate Domain Wall Spin-Orbit Torque Device. <i>Advanced Intelligent Systems</i> , 2022, 4, .	6.1	13
20	Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. <i>IEEE Transactions on Device and Materials Reliability</i> , 2011, 11, 378-386.	2.0	12
21	Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. <i>IEEE Transactions on Electron Devices</i> , 2014, 61, 3345-3349.	3.0	11
22	Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. <i>IEEE Transactions on Electron Devices</i> , 2014, 61, 3296-3302.	3.0	11
23	A Dual Magnetic Tunnel Junction-Based Neuromorphic Device. <i>Advanced Intelligent Systems</i> , 2020, 2, 2000143.	6.1	11
24	Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 4687-4693.	3.0	8
25	Reconfigurable Physical Unclonable Function Based on Spin-Orbit Torque Induced Chiral Domain Wall Motion. <i>IEEE Electron Device Letters</i> , 2021, 42, 597-600.	3.9	8
26	MuGFET carrier mobility and velocity: Impacts of fin aspect ratio, orientation and stress. , 2010, , .		7
27	First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. <i>IEEE Transactions on Electron Devices</i> , 2012, 59, 2273-2276.	3.0	7
28	NEM relay design for compact, ultra-low-power digital logic circuits. , 2014, , .		7
29	Comprehensive understanding of hot carrier degradation in multiple-fin SOI FinFETs. , 2015, , .		7
30	Study of High-Performance Ge pMOSFET Scaling Accounting for Direct Source-to-Drain Tunneling. <i>IEEE Transactions on Electron Devices</i> , 2011, 58, 2895-2902.	3.0	6
31	Fabrication of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{\text{ON}}$ and Reduced Layout-Width Dependence. <i>IEEE Transactions on Electron Devices</i> , 2013, 60, 153-158.	3.0	6
32	Complementary Graphene-Ferroelectric Transistors (C-GFTs) as Synapses with Modulatable Plasticity for Supervised Learning. , 2019, , .		6
33	An Euler-Lagrange Equation Oriented Solution for Write Energy Minimization of STT-MRAM. <i>IEEE Transactions on Electron Devices</i> , 2019, 66, 3686-3689.	3.0	5
34	Memristors: A Spin-Orbit Torque Memristive Device ( <i>Adv. Electron. Mater.</i> 4/2019). <i>Advanced Electronic Materials</i> , 2019, 5, 1970022.	5.1	4
35	Complementary Memtransistor-Based Multilayer Neural Networks for Online Supervised Learning Through (Anti-)Spike-Timing-Dependent Plasticity. <i>IEEE Transactions on Neural Networks and Learning Systems</i> , 2022, 33, 6640-6651.	11.3	4
36	Effect of measurement speed ( $\sim 1/4\text{s}$ -800 ps) on the characterization of reliability behaviors for FDSOI nMOSFETs. , 2018, , .		3

#	ARTICLE	IF	CITATIONS
37	Thermally Assisted Skyrmion Memory (TA-SKM). IEEE Electron Device Letters, 2020, 41, 932-935.	3.9	3
38	Exploring the Designs of p-Type Piezoelectric FinFETs Based on NEGF Transport Simulations Comprising Phonon Scattering. IEEE Transactions on Electron Devices, 2019, 66, 4982-4988.	3.0	2
39	Piezoelectric Tunnel FET With a Steep Slope. IEEE Electron Device Letters, 2020, 41, 948-951.	3.9	2
40	Predictive Compact Modeling for Strain Effects in Nanoscale Transistors. , 2009, , .		1
41	Effectiveness of strained-Si technology for thin-body MOSFETs. , 2012, , .		1
42	Nano-scaled transistor reliability characterization at nano-second regime. Science China Information Sciences, 2021, 64, 1.	4.3	1
43	Variation-aware study of BJT-based capacitorless DRAM cell scaling limit. , 2012, , .		0
44	Oxygen-inserted SegFET: A candidate for 10-nm node system-on-chip applications. , 2014, , .		0
45	Ultra-Low Power Nano-electromechanical Switch Realized by Controlled and Reversible Crack. , 2018, , .		0