Zhiqiang You

List of Publications by Year in descending order

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1478505 1281871 12 140 11 6 citations h-index g-index papers 12 12 12 106 docs citations times ranked citing authors all docs

#	Article	IF	CITATIONS
1	Defect Analysis and Parallel Testing for 3D Hybrid CMOS-Memristor Memory. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 745-758.	4.6	6
2	Fault Modeling and Efficient Testing of Memristor-Based Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4444-4455.	5.4	16
3	Integrating Two Logics Into One Crossbar Array for Logic Gate Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2987-2991.	3.0	4
4	A high-performance CNN method for offline handwritten Chinese character recognition and visualization. Soft Computing, 2020, 24, 7977-7987.	3.6	46
5	A novel memristor-based restricted Boltzmann machine for contrastive divergence. IEICE Electronics Express, 2018, 15, 20171062-20171062.	0.8	7
6	Defect Analysis and Parallel March Test Algorithm for 3D Hybrid CMOS-Memristor Memory. , 2018, , .		5
7	Logic operationâ€based Design for Testability method and parallel test algorithm for 1T1R crossbar. Electronics Letters, 2017, 53, 1631-1632.	1.0	11
8	Efficient March test algorithm for 1T1R crossâ€bar with complete fault coverage. Electronics Letters, 2016, 52, 1520-1522.	1.0	20
9	A parallel-SSHI rectifier for ultra-low-voltage piezoelectric vibration energy harvesting. IEICE Electronics Express, 2016, 13, 20160539-20160539.	0.8	5
10	A signal degradation reduction method for memristor ratioed logic (MRL) gates. IEICE Electronics Express, 2015, 12, 20150062-20150062.	0.8	5
11	Logic operation-based DFT method and 1R memristive crossbar March-like test algorithm. IEICE Electronics Express, 2015, 12, 20150839-20150839.	0.8	9
12	An adaptive neural network A/D converter based on CMOS/memristor hybrid design. IEICE Electronics Express, 2014, 11, 20141012-20141012.	0.8	6