Zhiqiang You

List of Publications by Year
in descending order

12 papers	140 citations	1478505 6 h-index	1281871 11 g-index
12 all docs	12 docs citations	12 times ranked	106 citing authors

#	Article	IF	Citations
1	A high-performance CNN method for offline handwritten Chinese character recognition and visualization. Soft Computing, 2020, 24, 7977-7987.	3.6	46
2	Efficient March test algorithm for 1T1R crossâ€bar with complete fault coverage. Electronics Letters, 2016, 52, 1520-1522.	1.0	20
3	Fault Modeling and Efficient Testing of Memristor-Based Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4444-4455.	5.4	16
4	Logic operationâ€based Design for Testability method and parallel test algorithm for 1T1R crossbar. Electronics Letters, 2017, 53, 1631-1632.	1.0	11
5	Logic operation-based DFT method and 1R memristive crossbar March-like test algorithm. IEICE Electronics Express, 2015, 12, 20150839-20150839.	0.8	9
6	A novel memristor-based restricted Boltzmann machine for contrastive divergence. IEICE Electronics Express, 2018, 15, 20171062-20171062.	0.8	7
7	An adaptive neural network A/D converter based on CMOS/memristor hybrid design. IEICE Electronics Express, 2014, 11, 20141012-20141012.	0.8	6
8	Defect Analysis and Parallel Testing for 3D Hybrid CMOS-Memristor Memory. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 745-758.	4.6	6
9	A signal degradation reduction method for memristor ratioed logic (MRL) gates. IEICE Electronics Express, 2015, 12, 20150062-20150062.	0.8	5
10	A parallel-SSHI rectifier for ultra-low-voltage piezoelectric vibration energy harvesting. IEICE Electronics Express, 2016, 13, 20160539-20160539.	0.8	5
11	Defect Analysis and Parallel March Test Algorithm for 3D Hybrid CMOS-Memristor Memory. , 2018, , .		5
12	Integrating Two Logics Into One Crossbar Array for Logic Gate Design. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2987-2991.	3.0	4