Akhilesh Jaiswal

List of Publications by Year in descending order

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Δκημές η Ινιςνάλι

#	Article	IF	CITATIONS
1	Towards spike-based machine intelligence with neuromorphic computing. Nature, 2019, 575, 607-617.	27.8	869
2	X-SRAM: Enabling In-Memory Boolean Computations in CMOS Static Random Access Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4219-4232.	5.4	182
3	8T SRAM Cell as a Multibit Dot-Product Engine for Beyond Von Neumann Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2556-2567.	3.1	93
4	IMAC: In-Memory Multi-Bit Multiplication and ACcumulation in 6T SRAM Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2521-2531.	5.4	67
5	Xcel-RAM: Accelerating Binary Neural Networks in High-Throughput SRAM Compute Arrays. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3064-3076.	5.4	65
6	Proposal for a Leaky-Integrate-Fire Spiking Neuron Based on Magnetoelectric Switching of Ferromagnets. IEEE Transactions on Electron Devices, 2017, 64, 1818-1824.	3.0	63
7	In-Memory Low-Cost Bit-Serial Addition Using Commodity DRAM Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 155-165.	5.4	54
8	Comprehensive Scaling Analysis of Current Induced Switching in Magnetic Memories Based on In-Plane and Perpendicular Anisotropies. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 120-133.	3.6	36
9	lsing computation based combinatorial optimization using spin-Hall effect (SHE) induced stochastic magnetization reversal. Journal of Applied Physics, 2017, 121, .	2.5	35
10	Energy Efficient Neural Computing: A Study of Cross-Layer Approximations. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 796-809.	3.6	32
11	Significance Driven Hybrid 8T-6T SRAM for Energy-Efficient Synaptic Storage in Artificial Neural Networks. , 2016, , .		24
12	Modeling and Design Space Exploration for Bit-Cells Based on Voltage-Assisted Switching of Magnetic Tunnel Junctions. IEEE Transactions on Electron Devices, 2016, 63, 3493-3500.	3.0	21
13	Area-Efficient Nonvolatile Flip-Flop Based on Spin Hall Effect. IEEE Magnetics Letters, 2018, 9, 1-4.	1.1	21
14	MESL: Proposal for a Non-volatile Cascadable Magneto-Electric Spin Logic. Scientific Reports, 2017, 7, 39793.	3.3	19
15	In-situ, In-Memory Stateful Vector Logic Operations based on Voltage Controlled Magnetic Anisotropy. Scientific Reports, 2018, 8, 5738.	3.3	18
16	Designing Energy-Efficient Intermittently Powered Systems Using Spin-Hall-Effect-Based Nonvolatile SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 294-307.	3.1	18
17	<i>i-SRAM</i> : Interleaved Wordlines for Vector Boolean Operations Using SRAMs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4651-4659.	5.4	16
18	IMPULSE: A 65-nm Digital Compute-in-Memory Macro With Fused Weights and Membrane Potential for Spike-Based Sequential Learning Tasks. IEEE Solid-State Circuits Letters, 2021, 4, 137-140.	2.0	16

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#	Article	IF	CITATIONS
19	Energy-Efficient Memory Using Magneto-Electric Switching of Ferromagnets. IEEE Magnetics Letters, 2017, 8, 1-5.	1.1	10
20	CryoCiM: Cryogenic compute-in-memory based on the quantum anomalous Hall effect. Applied Physics Letters, 2022, 120, .	3.3	9
21	Design and Comparative Analysis of Spintronic Memories Based on Current and Voltage Driven Switching. IEEE Transactions on Electron Devices, 2018, 65, 2682-2693.	3.0	7
22	On Robustness of Spin-Orbit-Torque Based Stochastic Sigmoid Neurons for Spiking Neural Networks. , 2019, , .		7
23	Neural Computing With Magnetoelectric Domain-Wall-Based Neurosynaptic Devices. IEEE Transactions on Magnetics, 2021, 57, 1-9.	2.1	7
24	<i>In situ</i> unsupervised learning using stochastic switching in magneto-electric magnetic tunnel junctions. Philosophical Transactions Series A, Mathematical, Physical, and Engineering Sciences, 2020, 378, 20190157.	3.4	6
25	Robust and Cascadable Nonvolatile Magnetoelectric Majority Logic. IEEE Transactions on Electron Devices, 2017, 64, 5209-5216.	3.0	3
26	Functional Read Enabling In-Memory Computations in 1Transistor—1Resistor Memory Arrays. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3347-3351.	3.0	3
27	Spin transfer torque memories for on-chip caches: Prospects and perspectives. , 2016, , .		1
28	A non-volatile cascadable magneto-electric material implication logic. , 2017, , .		1
29	Stochastic Switching of SHE-MTJ as a Natural Annealer for Efficient Combinatorial Optimization. , 2017, , .		1
30	Capacitively Driven Global Interconnect With Energy-Efficient Receiver Based on Magneto-Electric Switching. IEEE Magnetics Letters, 2018, 9, 1-5.	1.1	0