Taegeun Yoo

List of Publications by Year
in descending order

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23	432	1040056 9	940533 16
papers	citations	h-index	g-index

23	23	23	387
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 6T SRAM Based Two-Dimensional Configurable Challenge-Response PUF for Portable Devices. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2542-2552.	5.4	3
2	A 65-nm 8T SRAM Compute-in-Memory Macro With Column ADCs for Processing Neural Networks. IEEE Journal of Solid-State Circuits, 2022, 57, 3466-3476.	5.4	25
3	A Logic-Compatible eDRAM Compute-In-Memory With Embedded ADCs for Processing Neural Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 667-679.	5.4	35
4	Colonnade: A Reconfigurable SRAM-Based Digital Bit-Serial Compute-In-Memory Macro for Processing Neural Networks. IEEE Journal of Solid-State Circuits, 2021, 56, 2221-2233.	5.4	62
5	A 0.5 V 8â€“12 Bit 300 KSPS SAR ADC With Adaptive Conversion Time Detection-and-Control for High Immunity to PVT Variations. IEEE Access, 2020, 8, 101359-101368.	4.2	7
6	A 16K Current-Based 8T SRAM Compute-In-Memory Macro with Decoupled Read/Write and 1-5bit Column ADC. , 2020, , .		65
7	SRAM Radiation Hardening Through Self-Refresh Operation and Error Correction. IEEE Transactions on Device and Materials Reliability, 2020, 20, 468-474.	2.0	11
8	A 0.506-pJ 16-kb 8T SRAM With Vertical Read Wordlines and Selective Dual Split Power Lines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1345-1356.	3.1	9
9	A 16Ã—128 Stochastic-Binary Processing Element Array for Accelerating Stochastic Dot-Product Computation Using 1-16 Bit-Stream Length. , 2020, , .		2
10	A 137-Î¼W 1.78-mm² 30-Frames/s Real-Time Gesture Recognition SoC for Smart Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1909-1919.	3.1	2
11	Design of Current-Mode 8T SRAM Compute-In-Memory Macro for Processing Neural Networks. , 2020, , .		0
12	A Low-Power Smart Gesture Sensing SoC with On-chip Image Sensor for Smart Devices. , 2020, , .		0
13	A Logic Compatible 4T Dual Embedded DRAM Array for In-Memory Computation of Deep Neural Networks. , 2019, , .		17
14	A 213.7-mu W Gesture Sensing System-On-Chip With Self-Adaptive Motion Detection and Noise-Tolerant Outermost-Edge-Based Feature Extraction in 65 nm. IEEE Solid-State Circuits Letters, 2019, 2, 123-126.	2.0	7
15	Balanced sampling switch for high linearity and a wide temperature range in low power SAR ADCs. Electronics Letters, 2019, 55, 1273-1275.	1.0	3
16	A 1-16b Precision Reconfigurable Digital In-Memory Computing Macro Featuring Column-MAC Architecture and Bit-Serial Computation. , 2019, , .		38
17	A 0.016 mV/mA Cross-Regulation 5-Output SIMO DCâ€“DC Buck Converter Using Output-Voltage-Aware Charge Control Scheme. IEEE Transactions on Power Electronics, 2018, 33, 9619-9630.	7.9	28
18	An Ultra-low Power 8T SRAM with Vertical Read Word Line and Data Aware Write Assist. , 2018, , .		9

#	Article	IF	Citations
19	An 88% Efficiency 0.1â€“300-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>W Energy Harvesting System With 3-D MPPT Using Switch Width Modulation for IoT Smart Nodes. IEEE Journal of Solid-State Circuits, 2018, 53, 2751-2762.	5.4	53
20	A 12-bit Multi-Channel R-R DAC Using a Shared Resistor String Scheme for Area-Efficient Display Source Driver. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3688-3697.	5.4	16
21	A 2 GHz 130 mW Direct-Digital Frequency Synthesizer With a Nonlinear DAC in 55 nm CMOS. IEEE Journal of Solid-State Circuits, 2014, 49, 2976-2989.	5.4	30
22	Pipelined phase accumulator using sequential FCW loading scheme for DDFSs. Electronics Letters, 2012, 48, 1044-1046.	1.0	7
23	Low-power fast-update pipelined phase accumulator for CML-based high-speed CMOS DDFSs. Electronics Letters, 2012, 48, 1102-1104.	1.0	3