Robert Bogdan Staszewski

List of Publications by Year
in descending order

362	8,764	71061	69214
papers	citations	41 h-index	77 g-index

385	385	385	3571
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 20 MHzâ€“2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 42-50.	3.5	22
2	A Compact 0.2â€“0.3-V Inverse-Class-F₂₃ Oscillator for Low 1/f ³ Noise Over Wide Tuning Range. IEEE Journal of Solid-State Circuits, 2022, 57, 452-464.	3.5	7
3	A Charge-Sharing Locking Technique With a General Phase Noise Theory of Injection Locking. IEEE Journal of Solid-State Circuits, 2022, 57, 518-534.	3.5	12
4	A Broadband Fully Integrated Power Amplifier Using Waveform Shaping Multi-Resonance Harmonic Matching Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2-15.	3.5	13
5	Mismatch Analysis of DTCs With an Improved BIST-TDC in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 196-206.	3.5	4
6	A Clock-Phase Reuse Technique for Discrete-Time Bandpass Filters. IEEE Journal of Solid-State Circuits, 2022, 57, 290-301.	3.5	2
7	A 529-Î¼W Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 51-63.	3.5	13
8	A Deep-Subthreshold Variation-Aware 0.2-V Open-Loop VCO-Based ADC. IEEE Journal of Solid-State Circuits, 2022, 57, 1684-1699.	3.5	12
9	Flicker Phase-Noise Reduction Using Gateâ€“Drain Phase Shift in Transformer-Based Oscillators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 973-984.	3.5	4
10	A Fractional-N Digitally Intensive PLL Achieving 428-fs Jitter and <â^'54-dBc Spurs Under 50-mVpp Supply Ripple. IEEE Journal of Solid-State Circuits, 2022, 57, 1749-1764.	3.5	5
11	Three-Winding Transformer-Based 60-GHz DCO With â^'185.1-dB FoM in 40-nm CMOS. IEEE Solid-State Circuits Letters, 2022, 5, 1-4.	1.3	4
12	A mm-Wave Switched-Capacitor RFDAC. IEEE Journal of Solid-State Circuits, 2022, 57, 1224-1238.	3.5	8
13	Topological order detection and qubit encoding in Suâ€“Schriefferâ€“Heeger type quantum dot arrays. Journal of Applied Physics, 2022, 131, .	1.1	6
14	A 2.6-to-4.1GHz Fractional-N Digital PLL Based on a Time-Mode Arithmetic Unit Achieving -249.4dB FoM and -59dBc Fractional Spurs. , 2022, , .		2
15	Multirate Timestamp Modeling for Ultralow-Jitter Frequency Synthesis: A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3030-3036.	2.2	4
16	A Charge-Sharing IIR Filter With Linear Interpolation and High Stopband Rejection. IEEE Journal of Solid-State Circuits, 2022, 57, 2090-2101.	3.5	4
17	Design of High-IF Discrete-Time Receivers for IoT: Demystifying Aliasing Trade-Offs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3078-3083.	2.2	1
18	A Fully Integrated GaN Dual-Channel Power Amplifier With Crosstalk Suppression for 5G Massive MIMO Transmitters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 246-250.	2.2	16

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19	A Type-II Phase-Tracking Receiver. IEEE Journal of Solid-State Circuits, 2021, 56, 427-439.	3.5	12
20	Oscillator Flicker Phase Noise: A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 538-544.	2.2	25
21	Dickson-Charge-Pump-Based Voltage-to-Time Conversion for Time-Based ADCs in 28-nm CMOS. IEEE Open Journal of Circuits and Systems, 2021, 2, 23-31.	1.4	10
22	Unbalanced Power Amplifier: An Architecture for Broadband Back-Off Efficiency Enhancement. IEEE Journal of Solid-State Circuits, 2021, 56, 367-381.	3.5	15
23	A 0.02â€“4.5-GHz LN(T)A in 28-nm CMOS for 5G Exploiting Noise Reduction and Current Reuse. IEEE Journal of Solid-State Circuits, 2021, 56, 404-415.	3.5	45
24	Correction to â€œA 32â€“42-GHz RTWO-Based Frequency Quadrupler Achieving >37 dBc Harmonic Rejection in 22-nm FD-SOIâ€. IEEE Solid-State Circuits Letters, 2021, 4, 104-104.	1.3	0
25	Towards the Co-Simulation of Charge Qubits: A Methodology Grounding on an Equivalent Circuit Representation. IEEE Open Journal of Circuits and Systems, 2021, 2, 548-563.	1.4	2
26	A 32â€“42-GHz RTWO-Based Frequency Quadrupler Achieving >37 dBc Harmonic Rejection in 22-nm FD-SOI. IEEE Solid-State Circuits Letters, 2021, 4, 72-75.	1.3	7
27	An Active-Under-Coil RFDAC With Analog Linear Interpolation in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1855-1868.	3.5	1
28	A Reference-Waveform Oversampling Technique in a Fractional-N ADPLL. IEEE Journal of Solid-State Circuits, 2021, 56, 3445-3457.	3.5	10
29	Cryo-CMOS for Quantum System On-Chip Integration: Quantum Computing as the Development Driver. IEEE Solid-State Circuits Magazine, 2021, 13, 46-53.	0.5	14
30	A Low Profile Highly Isolated Phased Array MIMO Antenna System for 5G Applications at 28 GHz. , 2021, , .		1
31	A 0.7-V Sub-mW Type-II Phase-Tracking Bluetooth Low Energy Receiver in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2317-2328.	3.5	5
32	A 24â€“31 GHz Reference Oversampling ADPLL Achieving FoM_{jitterâ€²N} of -269.3 dB. , 2021, , .		4
33	A Distributed Stubs Technique to Mitigate Flicker Noise Upconversion in a mm-Wave Rotary Traveling-Wave Oscillator. IEEE Journal of Solid-State Circuits, 2021, 56, 1745-1760.	3.5	3
34	CMOS charge qubits and qudits: entanglement entropy and mutual information as an optimization method to construct CNOT and SWAP Gates. Semiconductor Science and Technology, 2021, 36, 095014.	1.0	6
35	A 38.6-fJ/Conv.-Step Inverter-Based Continuous-Time Bandpass Î”Î£ ADC in 28 nm Using Asynchronous SAR Quantizer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3113-3117.	2.2	4
36	A Compact Transformer-Based Fractional-N ADPLL in 10-nm FinFET CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1881-1891.	3.5	5

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37	Interchannel Mismatch Calibration Techniques for Time-Interleaved SAR ADCs. IEEE Open Journal of Circuits and Systems, 2021, 2, 420-433.	1.4	2
38	Semiconductor Quantum Computing: Toward a CMOS quantum computer on chip. IEEE Nanotechnology Magazine, 2021, 15, 8-20.	0.9	10
39	A 28-GHz Switched-Filter Phase Shifter with Fine Phase-Tuning Capability Using Back-Gate Biasing in 22-nm FD-SOI CMOS. , 2021, , .		2
40	A Charge-Rotating IIR Filter with Linear Interpolation and High Stop-Band Rejection. , 2021, , .		2
41	A Millimeter-Wave ADPLL With Reference Oversampling and Third-Harmonic Extraction Featuring High FoM_{jitter-N}. IEEE Solid-State Circuits Letters, 2021, 4, 214-217.	1.3	6
42	Cryogenic Low-Drop-Out Regulators Fully Integrated with Quantum Dot Array in 22-nm FD-SOI CMOS. , 2021, , .		3
43	A 55.9-fs Integrated Jitter (100 kHzâ€“100 MHz) Hybrid LC-Tank PLL in 5-nm FinFET Using Programmable Phase Realignment and Dynamic Coarse Tuning. IEEE Solid-State Circuits Letters, 2021, 4, 230-233.	1.3	2
44	Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 37-41.	2.2	4
45	Passive SC $DeltaSigma$ Modulator Based on Pipelined Charge-Sharing Rotation in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 578-589.	3.5	5
46	An Event-Driven Quasi-Level-Crossing Delta Modulator Based on Residue Quantization. IEEE Journal of Solid-State Circuits, 2020, 55, 298-311.	3.5	19
47	CMOS Position-Based Charge Qubits: Theoretical Analysis of Control and Entanglement. IEEE Access, 2020, 8, 4182-4197.	2.6	24
48	Position-Based CMOS Charge Qubits for Scalable Quantum Processors at 4K. , 2020, , .		9
49	A Hybrid-PLL (ADPLL/Charge-Pump PLL) Using Phase Realignment With 0.6-us Settling, 0.619-ps Integrated Jitter, and â^'240.5-dB FoM in 7-nm FinFET. IEEE Solid-State Circuits Letters, 2020, 3, 174-177.	1.3	8
50	A Tiny Complementary Oscillator With 1/f ³ Noise Reduction Using a Triple-8-Shaped Transformer. IEEE Solid-State Circuits Letters, 2020, 3, 162-165.	1.3	13
51	A Switched-Capacitor DC-DC Converter Powering an LC Oscillator to Achieve 85% System Peak Power Efficiency and â^'65dBc Spurious Tones. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3764-3777.	3.5	1
52	A Fully Integrated Reconfigurable Multimode Class-F_{2,3} GaN Power Amplifier. IEEE Solid-State Circuits Letters, 2020, 3, 270-273.	1.3	2
53	A Single-Electron Injection Device for CMOS Charge Qubits Implemented in 22-nm FD-SOI. IEEE Solid-State Circuits Letters, 2020, 3, 206-209.	1.3	21
54	Towards quantum internet and non-local communication in position-based qubits. AIP Conference Proceedings, 2020, , .	0.3	6

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55	Time-Domain Multiply-Accumulator using Digital-to-Time Multiplier for CNN Processors in 28-nm CMOS. , 2020, , .		0
56	A Fully Integrated DAC for CMOS Position-Based Charge Qubits with Single-Electron Detector Loopback Testing. IEEE Solid-State Circuits Letters, 2020, 3, 354-357.	1.3	15
57	Electrostatic Control and Entanglement of CMOS Position-Based Qubits. , 2020, , .		0
58	17.6 A 21.7-to-26.5GHz Charge-Sharing Locking Quadrature PLL with Implicit Digital Frequency-Tracking Loop Achieving 75fs Jitter and â˜’250dB FoM. , 2020, , .		27
59	A 0.2-V Three-Winding Transformer-Based DCO in 16-nm FinFET CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2878-2882.	2.2	10
60	A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Pushâ€“Pull LNA. IEEE Journal of Solid-State Circuits, 2020, 55, 2055-2068.	3.5	9
61	A Mismatch Calibration Technique for SAR ADCs Based on Deterministic Self-Calibration and Stochastic Quantization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2883-2896.	3.5	16
62	Broadband Fully Integrated GaN Power Amplifier With Minimum-Inductance BPF Matching and Two-Transistor AM-PM Compensation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4211-4223.	3.5	18
63	A 2.02â€“2.87-GHz â˜’249-dB FoM 1.1-mW Digital PLL Exploiting Reference-Sampling Phase Detector. IEEE Solid-State Circuits Letters, 2020, 3, 158-161.	1.3	11
64	Analytical solutions for N interacting electron system confined in graph of coupled electrostatic semiconductor and superconducting quantum dots in tight-binding model. Cryogenics, 2020, 109, 103117.	0.9	8
65	Breaking the Bandwidth Limit: A Review of Broadband Doherty Power Amplifier Design for 5G. IEEE Microwave Magazine, 2020, 21, 57-75.	0.7	60
66	A 0.36-V 5-MS/s Time-Mode Flash ADC With Dickson-Charge-Pump-Based Comparators in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1789-1802.	3.5	20
67	An Adaptive-Resolution Quasi-Level-Crossing Delta Modulator With VCO-Based Residue Quantizer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2828-2832.	2.2	7
68	A Time-Domain 147fs_{rms 2.5}-MHz Bandwidth Two-Step Flash-MASH 1-1-1 Time-to-Digital Converter With Third-Order Noise-Shaping and Mismatch Correction. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2532-2545.	3.5	11
69	Simulation Methodology for Electron Transfer in CMOS Quantum Dots. Lecture Notes in Computer Science, 2020, , 650-663.	1.0	5
70	Modeling of Semiconductor Electrostatic Qubits Realized Through Coupled Quantum Dots. IEEE Access, 2019, 7, 49262-49278.	2.6	23
71	A 0.3V, 35% Tuning-Range, 60kHz 1/f³-Corner Digitally Controlled Oscillator with Vertically Integrated Switched Capacitor Banks Achieving FoM_T of -199dB in 28-nm CMOS. , 2019, , .		10
72	Broadband Fully Integrated GaN Power Amplifier With Embedded Minimum Inductor Bandpass Filter and AMâ€“PM Compensation. IEEE Solid-State Circuits Letters, 2019, 2, 159-162.	1.3	9

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73	Synchronization-Phase Alignment of All-Digital Phase-Locked Loop Chips for a 60-GHz MIMO Transmitter and Evaluation of Phase Noise Effects. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 3187-3199.	2.9	4
74	Bandwidth Enhancement of GaN MMIC Doherty Power Amplifiers Using Broadband Transformer-Based Load Modulation Network. IEEE Access, 2019, 7, 119844-119855.	2.6	34
75	A 184.6-dBc/Hz FoM 100-kHz Flicker Phase Noise Corner 30-GHz Rotary Traveling-Wave Oscillator Using Distributed Stubs in 22-nm FD-SOI. IEEE Solid-State Circuits Letters, 2019, 2, 103-106.	1.3	8
76	A 31-mu W, 148-fs Step, 9-bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 3075-3085.	3.5	24
77	Intuitive Understanding of Flicker Noise Reduction via Narrowing of Conduction Angle in Voltage-Biased Oscillators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1962-1966.	2.2	22
78	A 1-V Bandgap Reference in 7-nm FinFET With a Programmable Temperature Coefficient and Inaccuracy of Â±0.2% From â˜45Â°C to 125Â°C. IEEE Journal of Solid-State Circuits, 2019, 54, 1830-1840.	3.5	20
79	Design of Highly Linear Broadband Continuous Mode GaN MMIC Power Amplifiers for 5G. IEEE Access, 2019, 7, 57138-57150.	2.6	28
80	A 0.85mm² 51%-Efficient 11-dBm Compact DCO-DPA in 16-nm FinFET for Sub-Gigahertz IoT TX Using HD₂ Self-Suppression and Pulling Mitigation. IEEE Journal of Solid-State Circuits, 2019, 54, 2028-2037.	3.5	4
81	Challenges in On-Chip Antenna Design and Integration With RF Receiver Front-End Circuitry in Nanoscale CMOS for 5G Communication Systems. IEEE Access, 2019, 7, 43190-43204.	2.6	42
82	Photon Enhanced Interaction and Entanglement in Semiconductor Position-Based Qubits. Applied Sciences (Switzerland), 2019, 9, 4534.	1.3	10
83	A Verilog-A Model of the Shuttle of an Electron in a Two Quantum-Dot System. , 2019, , .		3
84	Two-Fold Noise-Cancelling Low-Noise Amplifier in 28-nm CMOS. , 2019, , .		1
85	DTC-Assisted All-Digital Phase-Locked Loop Exploiting Hybrid Time/Voltage Phase Digitization. , 2019, , .		0
86	A Python-Verilog Toolbox for Modeling of a Hadamard Gate Based on Position-Based CMOS Qubits. , 2019, , .		1
87	28 GHz Quadrature Frequency Generation Exploiting Injection-Locked Harmonic Extractors for 5G Communications. , 2019, , .		1
88	Analytic view on coupled single-electron lines. Semiconductor Science and Technology, 2019, 34, 125015.	1.0	10
89	A 184.6-dBc/Hz FoM 100-kHz Flicker Phase Noise Corner 30-GHz Rotary Traveling-Wave Oscillator Using Distributed Stubs in 22-nm FD-SOI. , 2019, , .		0
90	A Mixed-Signal Control Core for a Fully Integrated Semiconductor Quantum Computer System-on-Chip. , 2019, , .		37

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91	A 77/79-GHz Frequency Generator in 16-nm CMOS for FMCW Radar Applications Based on a 26-GHz Oscillator with Co-Generated Third Harmonic. , 2019, , .		5
92	A Broadband Continuous Class-FGaN MMIC PA Using Multi-Resonance Matching Network. , 2019, , .		7
93	Broadband Fully Integrated GaN Power Amplifier With Embedded Minimum Inductor Bandpass Filter and AMâ€“PM Compensation. , 2019, , .		0
94	A Low-Noise Fractional-<inline-formula> <tex-math notation="LaTeX">${N}$ </tex-math> </inline-formula> Digital Frequency Synthesizer With Implicit Frequency Tripling for mm-Wave Applications. IEEE Journal of Solid-State Circuits, 2019, 54, 755-767.	3.5	42
95	Design and Analysis of a DCO-Based Phase-Tracking RF Receiver for IoT Applications. IEEE Journal of Solid-State Circuits, 2019, 54, 785-795.	3.5	18
96	A Supply Pushing Reduction Technique for <italic>LC</italic> Oscillators Based on Ripple Replication and Cancellation. IEEE Journal of Solid-State Circuits, 2019, 54, 240-252.	3.5	12
97	From two types of electrostatic position-dependent semiconductor qubits to quantum universal gates and hybrid semiconductor-superconducting quantum computer. , 2019, , .		12
98	Energy-Efficient Wide-Range Voltage Level Shifters Reaching 4.2 fJ/Transition. IEEE Solid-State Circuits Letters, 2018, 1, 34-37.	1.3	49
99	Design procedure of a U-slot patch antenna array for 60 GHz MIMO application. , 2018, , .		2
100	A Low-Flicker-Noise 30-GHz Class-F₂₃ Oscillator in 28-nm CMOS Using Implicit Resonance and Explicit Common-Mode Return Path. IEEE Journal of Solid-State Circuits, 2018, 53, 1977-1987.	3.5	101
101	A 0.45V sub-mW all-digital PLL in 16nm FinFET for bluetooth low-energy (BLE) modulation and instantaneous channel hopping using 32.768kHz reference. , 2018, , .		6
102	A 4.4mW-TX, 3.6 mW-RX Fully Integrated Bluetooth Low Energy Transceiver for IoT Applications. , 2018, , 335-359.		0
103	Cryo-CMOS Circuits and Systems for Quantum Computing Applications. IEEE Journal of Solid-State Circuits, 2018, 53, 309-321.	3.5	276
104	An Adaptive-Resolution Quasi-Level-Crossing-Sampling ADC Based on Residue Quantization in 28-nm CMOS. IEEE Solid-State Circuits Letters, 2018, 1, 178-181.	1.3	6
105	A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS. IEEE Solid-State Circuits Letters, 2018, 1, 190-193.	1.3	24
106	Occupancy Oscillations and Electron Transfer in Multiple-Quantum-Dot Qubits and their Circuit Representation. , 2018, , .		4
107	Effects of Subharmonics in LO Generation on RF Transceivers. , 2018, , .		5
108	A 180 mV 81.2%-Efficient Switched-Capacitor Voltage Doubler for IoT Using Self-Biasing Deep N-Well in 16-nm CMOS FinFET. IEEE Solid-State Circuits Letters, 2018, 1, 158-161.	1.3	7

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109	A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA. , 2018, , .		3
110	A mm-Wave MIMO Transmitter with a Digital Beam Steering Capability Using CMOS All-Digital Phase-Locked Loop Chips. , 2018, , .		3
111	BJT Device and Circuit Co-Optimization Enabling Bandgap Reference and Temperature Sensing in 7-nm FinFET. , 2018, , .		7
112	All-Digital PLL for Bluetooth Low Energy Using 32.768-kHz Reference Clock and â‰0.45-V Supply. IEEE Journal of Solid-State Circuits, 2018, 53, 3660-3671.	3.5	25
113	A 0.2GHz to 4GHz Hybrid PLL (ADPLL/Charge-Pump-PLL) in 7NM FinFET CMOS Featuring 0.619PS Integrated Jitter and 0.6US Settling Time at 2.3MW. , 2018, , .		6
114	A 1 V Bandgap Reference in 7-nm FinFET with a Programmable Temperature Coefficient and an Inaccuracy of Â±0.2% from â^'45Â°C to 125Â°C. , 2018, , .		6
115	An On-Chip Self-Characterization of a Digital-to-Time Converter by Embedding it in a First-Order <inline-formula> <tex-math notation="LaTeX">$DeltaSigma$ </tex-math> </inline-formula> Loop. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3734-3744.	3.5	4
116	An All-Digital PLL for Cellular Mobile Phones in 28-nm CMOS with â^'55 dBc Fractional and â^'91 dBc Reference Spurs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3756-3768.	3.5	15
117	The (R)evolution of Distributed Amplifiers: From Vacuum Tubes to Modern CMOS and GaN ICs. IEEE Microwave Magazine, 2018, 19, 66-83.	0.7	41
118	A 0.5-V 1.6-mW 2.4-GHz Fractional-N All-Digital PLL for Bluetooth LE With PVT-Insensitive TDC Using Switched-Capacitor Doubler in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 2572-2583.	3.5	34
119	A 33-GHz LNA for 5G Wireless Systems in 28-nm Bulk CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1460-1464.	2.2	68
120	A low cost-low loss broadband integration of a CMOS transmitter and its antenna for mm-wave FMCW radar applications. AEU - International Journal of Electronics and Communications, 2018, 95, 313-325.	1.7	5
121	Towards Ultra-Low-Voltage and Ultra-Low-Power Discrete-Time Receivers for Internet-of-Things. , 2018, , .		3
122	Numerical Model of an Injection-Locked Wideband Frequency Modulator for Polar Transmitters. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 1914-1920.	2.9	4
123	A Bluetooth Low-Energy Transceiver With 3.7-mW All-Digital Transmitter, 2.75-mW High-IF Discrete-Time Receiver, and TX/RX Switchable On-Chip Matching Network. IEEE Journal of Solid-State Circuits, 2017, 52, 1144-1162.	3.5	95
124	15.5 Cryo-CMOS circuits and systems for scalable quantum computing. , 2017, , .		53
125	19.6 A 0.2V trifilar-coil DCO with DC-DC converter in 16nm FinFET CMOS with 188dB FOM, 1.3kHz resolution, and frequency pushing of 38MHz/V for energy harvesting applications. , 2017, , .		13
126	24.1 A 770pJ/b 0.85V 0.3mm² DCO-based phase-tracking RX featuring direct demodulation and data-aided carrier tracking for IoT applications. , 2017, , .		8

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127	A 3.5â€“6.8-GHz Wide-Bandwidth DTC-Assisted Fractional-N All-Digital PLL With a MASH $Delta Sigma $ -TDC for Low In-Band Phase Noise. IEEE Journal of Solid-State Circuits, 2017, 52, 1885-1903.	3.5	62
128	An Ultracompact 9.4â€“14.8-GHz Transformer-Based Fractional-N All-Digital PLL in 40-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 4241-4254.	2.9	13
129	System Design of a 2.75-mW Discrete-Time Superheterodyne Receiver for Bluetooth Low Energy. IEEE Transactions on Microwave Theory and Techniques, 2017, 65, 1904-1913.	2.9	15
130	Tuning Range Extension of a Transformer-Based Oscillator Through Common-Mode Colpitts Resonance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 836-846.	3.5	23
131	An Ultra-Low Power 1.7-2.7 GHz Fractional-N Sub-Sampling Digital Frequency Synthesizer and Modulator for IoT Applications in 40 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1094-1105.	3.5	46
132	A 0.5V 1.6mW 2.4GHz fractional-N all-digital PLL for Bluetooth LE with PVT-insensitive TDC using switched-capacitor doubler in 28nm CMOS. , 2017, , .		2
133	Frequency-domain adaptive-resolution level-crossing-sampling ADC. , 2017, , .		1
134	Introduction to the Special Issue on the 46th European Solid-State Circuits Conference (ESSCIRC). IEEE Journal of Solid-State Circuits, 2017, 52, 1700-1702.	3.5	0
135	A Fully Integrated Discrete-Time Superheterodyne Receiver. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 635-647.	2.1	18
136	Oscillator-based ADCs: An exploration of time-mode analog-to-digital conversion. , 2017, , .		0
137	A 4GHz clock distribution architecture using subharmonically injection-locked coupled oscillators with clock skew calibration in 16nm CMOS. , 2017, , .		3
138	A 350-mV 2.4-GHz quadrature oscillator with nearly instantaneous start-up using series LC tanks. , 2017, , .		7
139	A 15-Î¼W, 103-fs step, 5-bit capacitor-DAC-based constant-slope digital-to-time converter in 28nm CMOS. , 2017, , .		5
140	A 30-GHz class-F23 oscillator in 28nm CMOS using harmonic extraction and achieving 120 kHz 1/f³ corner. , 2017, , .		5
141	Differential I/Q DPA and power-combining network. , 2017, , 173-200.		0
142	Future of RFDAC. , 2017, , 245-250.		0
143	Digital polar transmitter architecture. , 2017, , 21-40.		0
144	Simulation and measurement results of the polar transmitter. , 2017, , 117-127.		0

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145	RF front-end (RFDAC) of the polar transmitter. , 2017, , 77-116.		0
146	Toward high-resolution RFDAC. , 2017, , 161-171.		0
147	Orthogonal summation. , 2017, , 143-159.		0
148	Idea of all-digital I/Q modulator. , 2017, , 129-141.		0
149	Digital baseband of the polar transmitter. , 2017, , 41-76.		0
150	Measurement results of the 2 Ã— 13-bit I/Q RFDAC. , 2017, , 229-244.		0
151	A wideband 2 Ã— 13-bit all-digital I/Q RFDAC. , 2017, , 201-228.		0
152	Millimeter-Wave Digitally Controlled Oscillator. , 2016, , 81-106.		0
153	Design for Test of the mm-Wave ADPLL. , 2016, , 163-182.		0
154	All-Digital Phase-Locked Loop. , 2016, , 57-80.		0
155	A 38 GHz on-chip antenna in 28-nm CMOS using artificial magnetic conductor for 5G wireless systems. , 2016, , .		10
156	A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier. IEEE Journal of Solid-State Circuits, 2016, 51, 1261-1273.	3.5	108
157	A Fully Integrated Bluetooth Low-Energy Transmitter in 28 nm CMOS With 36% System Efficiency at 3 dBm. IEEE Journal of Solid-State Circuits, 2016, 51, 1547-1565.	3.5	66
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