Michael C Huang

List of Publications by Year
in descending order

86 papers	1,362 citations	687363 13 h-index	610901 24 g-index
86 all docs	86 docs citations	86 times ranked	1025 citing authors

#	Article	IF	Citations
1	HyBP: Hybrid Isolation-Randomization Secure Branch Predictor. , 2022, , .		2
2	Increasing ising machine capacity with multi-chip architectures. , 2022, , .		7
3	LoopIn: A Loop-Based Simulation Sampling Mechanism. , 2022, , .		1
4	Exploiting Security Dependence for Conditional Speculation Against Spectre Attacks. IEEE Transactions on Computers, 2021, 70, 963-978.	3.4	1
5	BRIM: Bistable Resistively-Coupled Ising Machine. , 2021, , .		16
6	A Lightweight Isolation Mechanism for Secure Branch Predictors. , 2021, , .		11
7	Portable ultrasound imaging system with super-resolution capabilities. Ultrasonics, 2019, 94, 391-400.	3.9	6
8	Bootstrapping. , 2019, , .		3
9	R3-DLA (Reduce, Reuse, Recycle): A More Efficient Approach to Decoupled Look-Ahead Architectures. , 2019, , .		6
10	Venice. ACM Transactions on Computer Systems, 2019, 36, 1-26.	0.8	11
11	Concurrent Multipoint-to-Multipoint Communication on Interposer Channels. , 2019, , .		0
12	To Stack or Not To Stack. , 2019, , .		1
13	A Case for a More Effective, Power-Efficient Turbo Boosting. Transactions on Architecture and Code Optimization, 2018, 15, 1-22.	2.0	15
14	Safety and cost efficiency of a restrictive transfusion protocol in patients with traumatic brain injury. Journal of Neurosurgery, 2018, 128, 1530-1537.	1.6	14
15	Bootstrapping: Using SMT Hardware to Improve Single-Thread Performance. IEEE Computer Architecture Letters, 2018, 17, 205-208.	1.5	2
16	High Swing Pulse-Amplitude Modulation of Transmission Line Links for On-Chip Communication. , 2018, , .		2
17	Division of Labor: A More Effective Approach to Prefetching. , 2018, , .		17
18	Hadoop Configuration Tuning With Ensemble Modeling and Metaheuristic Optimization. IEEE Access, 2018, 6, 44161-44174.	4.2	20

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19	Hardware support for protective and collaborative cache sharing. ACM SIGPLAN Notices, 2018, 51, 24-35.	0.2	0
20	T2: A Highly Accurate and Energy Efficient Stride Prefetcher. , 2017, , .		9
21	Redundant Memory Array Architecture for Efficient Selective Protection. , 2017, , .		4
22	DRUT: An Efficient Turbo Boost Solution via Load Balancing in Decoupled Look-Ahead Architecture. , 2017, , .		0
23	A 100-MHz 256b-I/O 1-Mb planar nonvolatile STT-MRAM with novel memory cells. , 2016, , .		1
24	Thread-Aware Adaptive Prefetcher on Multicore Systems. Transactions on Architecture and Code Optimization, 2016, 13, 1-25.	2.0	6
25	Heterogeneous 3-D circuits: Integrating free-space optics with CMOS. Microelectronics Journal, 2016, 50, 66-75.	2.0	8
26	Threads and Data Mapping: Affinity Analysis for Traffic Reduction. IEEE Computer Architecture Letters, 2016, 15, 133-136.	1.5	0
27	Venice: Exploring server architectures for effective resource sharing. , 2016, , .		10
28	Building Expressive and Area-Efficient Directories with Hybrid Representation and Adaptive Multi-Granular Tracking. IEEE Transactions on Computers, 2016, 65, 847-859.	3.4	0
29	Hardware support for protective and collaborative cache sharing. , 2016, , .		0
30	Load Balancing in Decoupled Look-ahead: A Do-It-Yourself (DIY) Approach. , 2015, , .		0
31	Exploiting Transmission Lines on Heterogeneous Networks-on-Chip to Improve the Adaptivity and Efficiency of Cache Coherence. , 2015, , .		2
32	Protection and utilization in shared cache through rationing. , 2014, , .		3
33	Accelerating decoupled look-ahead via weak dependence removal: A metaheuristic approach. , 2014, , .		5
34	DEAM: Decoupled, Expressive, Area-Efficient Metadata Cache. Journal of Computer Science and Technology, 2014, 29, 679-691.	1.5	1
35	Generating efficient data movement code for heterogeneous architectures with distributed-memory. , 2013, , .		2
36	Assessment of cloud-based health monitoring using Homomorphic Encryption. , 2013, , .		50

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37	Energy Efficient Run-Time Incremental Mapping for 3-D Networks-on-Chip. Journal of Computer Science and Technology, 2013, 28, 54-71.	1.5	22
38	A coldness metric for cache optimization. , 2013, , .		0
39	A 25-Gbps 8-ps/mm transmission line based interconnect for on-chip communications in multi-core chips. , 2013, , .		10
40	3-D integrated heterogeneous intra-chip free-space optical interconnect. Optics Express, 2012, 20, 4331.	3.4	46
41	Chip-scale demonstration of 3D integrated intrachip free-space optical interconnect. , 2012, , .		6
42	Enhancing effective throughput for transmission line-based bus. Computer Architecture News, 2012, 40, 165-176.	2.5	6
43	Using Transmission Lines for Global On-Chip Communication. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 183-193.	3.6	19
44	Recent progress on 3-D integrated intra-chip free-space optical interconnect. , 2012, , .		6
45	Enhancing effective throughput for transmission line-based bus. , 2012, , .		11
46	Nanospintronics Based on Magnetologic Gates. IEEE Transactions on Electron Devices, 2012, 59, 259-262.	3.0	141
47	A design space exploration of transmission-line links for on-chip interconnect. , 2011, , .		5
48	Efficient data streaming with on-chip accelerators: Opportunities and challenges. , 2011, , .		13
49	Speculative Parallelization in Decoupled Look-ahead. , 2011, , .		8
50	Spintronics search engines. , 2011, , .		0
51	POPS: Coherence Protocol Optimization for Both Private and Shared Data. , 2011, , .		32
52	A 3-D Integrated Intrachip Free-Space Optical Interconnect for Many-Core Chips. IEEE Photonics Technology Letters, 2011, 23, 164-166.	2.5	22
53	Particle-in-cell simulations with charge-conserving current deposition on graphic processing units. Journal of Computational Physics, 2011, 230, 1676-1685.	3.8	35
54	A case for globally shared-medium on-chip interconnect. Computer Architecture News, 2011, 39, 271-282.	2.5	3

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55	Low latency and energy efficient multicasting schemes for 3D NoC-based SoCs. , 2011, , .		11
56	Reconfigurable nanoelectronics using graphene based spintronic logic gates. Proceedings of SPIE, 2011, , .	0.8	6
57	A case for globally shared-medium on-chip interconnect. , 2011, , .		25
58	Power-Aware Run-Time Incremental Mapping for 3-D Networks-on-Chip. Lecture Notes in Computer Science, 2011, , 232-247.	1.3	4
59	An intra-chip free-space optical interconnect. Computer Architecture News, 2010, 38, 94-105.	2.5	14
60	An intra-chip free-space optical interconnect. , 2010, , .		45
61	Variation-tolerant hierarchical voltage monitoring circuit for soft error detection. , 2009, , .		18
62	DDCache: Decoupled and Delegable Cache Data and Metadata. , 2009, , .		9
63	Replacing Associative Load Queues: A Timing-Centric Approach. IEEE Transactions on Computers, 2009, 58, 496-511.	3.4	1
64	Supporting highly-decoupled thread-level redundancy for parallel programs. High Performance Computer Architecture (HPCA), Proceedings of the IEEE International Symposium on, 2008, , .	0.0	17
65	A performance-correctness explicitly-decoupled architecture. , 2008, , .		32
66	Injection-Locked Clocking: A Low-Power Clock Distribution Scheme for High-Performance Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1251-1256.	3.1	20
67	Improving support for locality and fine-grain sharing in chip multiprocessors. , 2008, , .		22
68	Substituting associative load queue with simple hash tables in out-of-order microprocessors. , 2006, , .		5
69	Slackened Memory Dependence Enforcement. Computer Architecture News, 2006, 34, 142-154.	2.5	7
70	SEED. , 2006, , .		6
71	Injection-Locked Clocking: A New GHz Clock Distribution Scheme. , 2006, , .		24
72	DMDC: Delayed Memory Dependence Checking through Age-Based Filtering. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	7

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73	A Load-Store Queue Design Based on Predictive State Filtering. Journal of Low Power Electronics, 2006, 2, 27-36.	0.6	5
74	Energy-aware fetch mechanism. , 2005, , .		6
75	Power-Efficient Error Tolerance in Chip Multiprocessors. IEEE Micro, 2005, 25, 60-70.	1.8	13
76	Exploiting coarse-grain verification parallelism for power-efficient fault tolerance. , 2005, , .		19
77	EXPERT. , 2004, , .		43
78	Dynamically tuning processor resources with adaptive processing. Computer, 2003, 36, 49-58.	1.1	127
79	Customizing the branch predictor to reduce complexity and energy consumption. IEEE Micro, 2003, 23, 12-25.	1.8	23
80	Branch prediction on demand. , 2003, , .		30
81	Energy-efficient hybrid wakeup logic. , 2002, , .		32
82	L1 data cache decomposition for energy efficiency. , 2001, , .		52
83	Positional adaptation of processors: application to energy reduction. , 0, , .		37
84	The Thrifty Barrier: Energy-Aware Synchronization in Shared-Memory Multiprocessors. , 0, , .		63
85	Software-Hardware Cooperative Memory Disambiguation. , 0, , .		9
86	Slackened Memory Dependence Enforcement: Combining Opportunistic Forwarding with Decoupled Verification. , 0, , .		9