

Hao Cai

List of Publications by Year in descending order

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papers

784
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76
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76
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76
times ranked

504
citing authors

#	ARTICLE	IF	CITATIONS
1	Compact Model of Dielectric Breakdown in Spin-Transfer Torque Magnetic Tunnel Junction. IEEE Transactions on Electron Devices, 2016, 63, 1762-1767.	1.6	132
2	Robust Ultra-Low Power Non-Volatile Logic-in-Memory Circuits in FD-SOI Technology. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 847-857.	3.5	85
3	A 22nm, 10.8 μm^2 /15.1 μm^2 Dual Computing Modes High Power-Performance-Area Efficiency Domained Background Noise Aware Keyword-Spotting Processor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4733-4746.	3.5	50
4	A 510-nW Wake-Up Keyword-Spotting Chip Using Serial-FFT-Based MFCC and Binarized Depthwise Separable CNN in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 151-164.	3.5	42
5	High Performance MRAM with Spin-Transfer-Torque and Voltage-Controlled Magnetic Anisotropy Effects. Applied Sciences (Switzerland), 2017, 7, 929.	1.3	40
6	Magnetic Tunnel Junction Applications. Sensors, 2020, 20, 121.	2.1	38
7	Multiplexing Sense-Amplifier-Based Magnetic Flip-Flop in a 28-nm FDSOI Technology. IEEE Nanotechnology Magazine, 2015, 14, 761-767.	1.1	31
8	Proposal of Analog In-Memory Computing With Magnified Tunnel Magnetoresistance Ratio and Universal STT-MRAM Cell. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1519-1531.	3.5	30
9	A Self-Timed Voltage-Mode Sensing Scheme With Successive Sensing and Checking for STT-MRAM. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1602-1614.	3.5	29
10	TG-SPP: A One-Transmission-Gate Short-Path Padding for Wide-Voltage-Range Resilient Circuits in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 1422-1436.	3.5	24
11	Precision Adaptive MFCC Based on R2SDF-FFT and Approximate Computing for Low-Power Speech Keywords Recognition. IEEE Circuits and Systems Magazine, 2021, 21, 24-39.	2.6	23
12	A survey of in-spin transfer torque MRAM computing. Science China Information Sciences, 2021, 64, 1.	2.7	22
13	Exploring Hybrid STT-MTJ/CMOS Energy Solution in Near-/Sub-Threshold Regime for IoT Applications. IEEE Transactions on Magnetics, 2018, 54, 1-9.	1.2	18
14	Stochastic computation with Spin Torque Transfer Magnetic Tunnel Junction. , 2015, , .		17
15	Low Power Magnetic Flip-Flop Optimization With FDSOI Technology Boost. IEEE Transactions on Magnetics, 2016, 52, 1-7.	1.2	13
16	A Wide-Voltage-Range Half-Path Timing Error-Detection System With a 9-Transistor Transition-Detector in 40-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2288-2297.	3.5	13
17	More is Less: Domain-Specific Speech Recognition Microprocessor Using One-Dimensional Convolutional Recurrent Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1571-1582.	3.5	13
18	Breakdown Analysis of Magnetic Flip-Flop With 28-nm UTBB FDSOI Technology. IEEE Transactions on Device and Materials Reliability, 2016, 16, 376-383.	1.5	11

#	ARTICLE	IF	CITATIONS
19	Addressing Failure and Aging Degradation in MRAM/MeRAM-on-FDSOI Integration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 239-250.	3.5	10
20	A Hierarchical Reliability Simulation Methodology for AMS Integrated Circuits and Systems. Journal of Low Power Electronics, 2012, 8, 697-705.	0.6	10
21	Toward Energy-Efficient STT-MRAM Design With Multi-Modes Reconfiguration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2633-2639.	2.2	9
22	A 1D-CRNN Inspired Reconfigurable Processor for Noise-robust Low-power Keywords Recognition. , 2021, , .		7
23	Cross-layer investigation of continuous-time sigma Δ modulator under aging effects. Microelectronics Reliability, 2015, 55, 645-653.	0.9	6
24	HTD: A Light-Weight Holoymmetrical Transition Detector for Wide-Voltage-Range Variation Resilient ICs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3907-3917.	3.5	6
25	Interplay Bitwise Operation in Emerging MRAM for Efficient In-memory Computing. CCF Transactions on High Performance Computing, 2020, 2, 282-296.	1.1	6
26	Reliability Analysis and Performance Evaluation of STT-MRAM-Based Physical Unclonable Function. Spin, 2020, 10, .	0.6	6
27	A Machine Learning Attack-Resilient Strong PUF Leveraging the Process Variation of MRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2712-2716.	2.2	6
28	A general cost-effective design structure for probabilistic-based noise-tolerant logic functions in nanometer CMOS technology. , 2013, , .		5
29	Efficient reliability evaluation methodologies for combinational circuits. Microelectronics Reliability, 2016, 64, 19-25.	0.9	5
30	Compressed Sensing for Wideband HF Channel Estimation. , 2018, , .		5
31	Enabling Resilient Voltage-Controlled MeRAM Using Write Assist Techniques. , 2018, , .		5
32	Voltage-Controlled Magnetic Anisotropy MeRAM Bit-Cell over Event Transient Effects. Journal of Low Power Electronics and Applications, 2019, 9, 15.	1.3	5
33	Investigation of PVT-Aware STT-MRAM Sensing Circuits for Low-VDD Scenario. Micromachines, 2021, 12, 551.	1.4	5
34	Self-compensation tensor multiplication unit for adaptive approximate computing in low-power CNN processing. Science China Information Sciences, 2022, 65, 1.	2.7	5
35	Correlation-Based Electromagnetic Analysis Attack Using Haar Wavelet Reconstruction with Low-Pass Filtering on an FPGA Implementaion of AES. , 2018, , .		4
36	Pj-AxMTJ: Process-in-memory with Joint Magnetization Switching for Approximate Computing in Magnetic Tunnel Junction. , 2019, , .		4

#	ARTICLE	IF	CITATIONS
37	MTJ-LRB: Proposal of MTJ-Based Loop Replica Bitline as MRAM Device-Circuit Interaction for PVT-Robust Sensing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3352-3356.	2.2	4
38	Commodity Bit-Cell Sponsored MRAM Interaction Design for Binary Neural Network. IEEE Transactions on Electron Devices, 2022, 69, 1721-1726.	1.6	4
39	Simulation study of aging in CMOS binary adders. , 2014, , .		3
40	Efficient computation of combinational circuits reliability based on probabilistic transfer matrix. , 2014, , .		3
41	Magnetic Tunnel Junction-based Analog-to-Digital Converter using Spin Orbit Torque Mechanism. , 2020, , .		3
42	Cryogenic In-MRAM Computing. , 2021, , .		3
43	Reliability Emphasized MTJ/CMOS Hybrid Circuit Towards Ultra-Low Power. , 2018, , .		2
44	Stability and Variability Emphasized STT-MRAM Sensing Circuit With Performance Enhancement. , 2018, , .		2
45	Reliability Aware AMS/RF Performance Optimization. Advances in Computer and Electrical Engineering Book Series, 2015, , 28-54.	0.2	2
46	A Modeling Attack Resilient Physical Unclonable Function Based on STT-MRAM. , 2020, , .		2
47	Efficient implementation for accurate analysis of CED circuits against multiple faults. , 2014, , .		1
48	A non-Monte-Carlo Methodology for Variability Analysis of Magnetic Tunnel Junction Based Circuits. IEEE Transactions on Magnetics, 2016, , 1-1.	1.2	1
49	Energy Efficient Magnetic Tunnel Junction Based Hybrid LSI Using Multi-Threshold UTBB-FD-SOI Device. , 2017, , .		1
50	Design Space Exploration of Magnetic Tunnel Junction based Stochastic Computing in Deep Learning. , 2018, , .		1
51	Nonlinear Functions in Learned Iterative Shrinkage-Thresholding Algorithm for Sparse Signal Recovery. , 2019, , .		1
52	Sparse Realization in Unreliable Spin-Transfer-Torque RAM for Convolutional Neural Network. IEEE Transactions on Magnetics, 2021, 57, 1-5.	1.2	1
53	Triple Sensing Current Margin for Maintainable MRAM Yield at Sub-100% Tunnel Magnetoresistance Ratio. IEEE Transactions on Magnetics, 2021, 57, 1-5.	1.2	1
54	Dependable STT-MRAM With Emerging Approximation and Speculation Paradigms. IEEE Design and Test, 2023, 40, 17-25.	1.1	1

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55	Magnetic Random-Access Memory-Based Approximate Computing: An overview. IEEE Nanotechnology Magazine, 2022, 16, 25-32.	0.9	1
56	A Novel In-MRAM Multiplier Using Toggle Spin Torques Switching. , 2020, , .		1
57	Quality Driven Systematic Approximation for Binary-Weight Neural Network Deployment. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2928-2940.	3.5	1
58	Hybrid MTJ-CMOS Integration for Sigma-Delta ADC. , 2021, , .		1
59	In-MRAM Computing Elements with Single-Step Convolution and Fully Connected for BNN/TNN. , 2021, , .		1
60	Bit-error-rate aware sensing-error correction interaction in spintronic MRAM. Journal of Systems Architecture, 2022, , 102557.	2.5	1
61	Triple-Skipping Near-MRAM Computing Framework for AIoT Era. , 2022, , .		1
62	A Target-Separable BWN Inspired Speech Recognition Processor with Low-power Precision-adaptive Approximate Computing. , 2022, , .		1
63	A fast reliability-aware approach for analogue integrated circuits based on Pareto fronts. , 2013, , .		0
64	A study of statistical variability-aware methods. , 2014, , .		0
65	Reliability-aware delay faults evaluation of CMOS flip-flops. , 2014, , .		0
66	Voltage-Controlled Magnetoelectric Memory Bit-cell Design With Assisted Body-bias in FD-SOI. , 2019, , .		0
67	Comprehensive Pulse Shape Induced Failure Analysis in Voltage-Controlled MRAM. , 2019, , .		0
68	A Self-Timing Voltage-Mode Sense Amplifier for STT-MRAM Sensing Yield Improvement. , 2019, , .		0
69	Ultra-low Power Access Strategy for Process-Voltage-Temperature Aware STT-MRAM. , 2021, , .		0
70	A Novel Hybrid Nonvolatile SRAM for Suppressing Leakage Power Using Tunnel FET. , 2021, , .		0
71	Multiplication Circuit Architecture for Error-Tolerant CNN-Based Keywords Speech Recognition. IEEE Design and Test, 2023, 40, 26-35.	1.1	0
72	Novel Self-timing Speculative Writing for Unreliable STT-MRAM. , 2020, , .		0

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73	A Self-regulating Dynamic Reference Sensing Scheme with Balanced Trade-Off between Read Disturbance and Sensing Margin. , 2021, , .		0
74	Modified Peripheral MRAM Sensing for In-memory Boolean Logic. , 2021, , .		0
75	Writing-only in-MRAM computing paradigm for ultra-low power applications. Microprocessors and Microsystems, 2022, 90, 104449.	1.8	0
76	Analytical Delay Model in Near-Threshold Domain Considering Transition Time. , 2021, , .		0