

Liang-Gee Chen

List of Publications by Year in descending order

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447
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7,042
citations

101384

36
h-index

114278

63
g-index

449
all docs

449
docs citations

449
times ranked

2312
citing authors

#	ARTICLE	IF	CITATIONS
1	Efficient moving object segmentation algorithm using background registration technique. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 577-586.	5.6	293
2	Analysis and architecture design of an HDTV720p 30 frames/s H.264/AVC encoder. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 673-688.	5.6	251
3	Analysis, fast algorithm, and VLSI architecture design for H.264/AVC intra frame coder. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 378-401.	5.6	245
4	Analysis and architecture design of variable block-size motion estimation for H.264/AVC. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 578-593.	0.1	209
5	Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform. IEEE Transactions on Signal Processing, 2004, 52, 1080-1089.	3.2	182
6	Analysis and architecture design of block-coding engine for EBCOT in JPEG 2000. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 219-230.	5.6	178
7	Analysis and complexity reduction of multiple reference frames motion estimation in H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 507-522.	5.6	151
8	An efficient and simple VLSI tree architecture for motion estimation algorithms. IEEE Transactions on Signal Processing, 1993, 41, 889-900.	3.2	129
9	Survey on Block Matching Motion Estimation Algorithms and Architectures with New Results. Journal of Signal Processing Systems, 2006, 42, 297-320.	1.0	128
10	An efficient architecture for two-dimensional discrete wavelet transform. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 536-545.	5.6	126
11	Error concealment of lost motion vectors with overlapped motion compensation. IEEE Transactions on Circuits and Systems for Video Technology, 1997, 7, 560-563.	5.6	122
12	Fast Video Segmentation Algorithm With Shadow Cancellation, Global Motion Compensation, and Adaptive Threshold Techniques. IEEE Transactions on Multimedia, 2004, 6, 732-748.	5.2	107
13	Level C+ data reuse scheme for motion estimation with corresponding coding orders. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 553-558.	5.6	102
14	A 1.3TOPS H.264/AVC single-chip encoder for HDTV applications. , 0, , .		89
15	Fast Algorithm and Architecture Design of Low-Power Integer Motion Estimation for H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 568-577.	5.6	85
16	A novel 2Dd-to-3D conversion system using edge information. IEEE Transactions on Consumer Electronics, 2010, 56, 1739-1745.	3.0	84
17	Motion adaptive interpolation with horizontal motion detection for deinterlacing. IEEE Transactions on Consumer Electronics, 2003, 49, 1256-1265.	3.0	82
18	A cost-effective architecture for 8 \times 8 two-dimensional DCT/IDCT using direct method. IEEE Transactions on Circuits and Systems for Video Technology, 1997, 7, 459-467.	5.6	80

#	ARTICLE	IF	CITATIONS
19	A new block-matching criterion for motion estimation and its implementation. IEEE Transactions on Circuits and Systems for Video Technology, 1995, 5, 231-236.	5.6	78
20	Generic RAM-based architectures for two-dimensional discrete wavelet transform with line-based method. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 910-920.	5.6	76
21	An efficient parallel motion estimation algorithm for digital image processing. IEEE Transactions on Circuits and Systems for Video Technology, 1991, 1, 378-385.	5.6	73
22	Fully utilized and reusable architecture for fractional motion estimation of H.264/AVC. , 0, , .		70
23	Parallel 4 \times 4 2D transform and inverse transform architecture for MPEG-4 AVC/H.264. , 0, , .		66
24	Global Elimination Algorithm and Architecture Design for Fast Block Matching Motion Estimation. IEEE Transactions on Circuits and Systems for Video Technology, 2004, 14, 898-907.	5.6	65
25	Analysis and VLSI architecture for 1-D and 2-D discrete wavelet transform. IEEE Transactions on Signal Processing, 2005, 53, 1575-1586.	3.2	65
26	Architecture design for deblocking filter in H.264/JVT/AVC. , 2003, , .		64
27	Efficient Depth Image Based Rendering with Edge Dependent Depth Filter and Interpolation. , 0, , .		64
28	A data-interlacing architecture with two-dimensional data-reuse for full-search block-matching algorithm. IEEE Transactions on Circuits and Systems for Video Technology, 1998, 8, 124-127.	5.6	63
29	Predictive watershed: a fast watershed algorithm for video segmentation. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 453-461.	5.6	63
30	Accuracy improvement and cost reduction of 3-step search block matching algorithm for video coding. IEEE Transactions on Circuits and Systems for Video Technology, 1994, 4, 88-90.	5.6	61
31	A single-chip CMOS APS camera with direct frame difference output. IEEE Journal of Solid-State Circuits, 1999, 34, 1415-1418.	3.5	60
32	Lifting based discrete wavelet transform architecture for JPEG2000. , 0, , .		60
33	A 212 MPixels/s 4096 \times 2160p Multiview Video Encoder Chip for 3D/Quad Full HDTV Applications. IEEE Journal of Solid-State Circuits, 2010, 45, 46-58.	3.5	60
34	Hardware-Efficient Belief Propagation. IEEE Transactions on Circuits and Systems for Video Technology, 2011, 21, 525-537.	5.6	60
35	Hardware architecture design for variable block size motion estimation in MPEG-4 AVC/JVT/ITU-T H.264. , 0, , .		58
36	System design consideration for digital wheelchair controller. IEEE Transactions on Industrial Electronics, 2000, 47, 898-907.	5.2	57

#	ARTICLE	IF	CITATIONS
37	Video de-interlacing by adaptive 4-field global/local motion compensated approach. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1569-1582.	5.6	55
38	Multimode Embedded Compression Codec Engine for Power-Aware Video Coding System. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 141-150.	5.6	54
39	Power-aware multimedia: concepts and design perspectives. IEEE Circuits and Systems Magazine, 2007, 7, 26-34.	2.6	50
40	Advances in Hardware Architectures for Image and Video Coding - A Survey. Proceedings of the IEEE, 2005, 93, 184-197.	16.4	48
41	Block-based Vanishing Line and Vanishing Point Detection for 3D Scene Reconstruction. , 2006, , .		48
42	Depth Map Generation for 2D-to-3D Conversion by Short-Term Motion Assisted Color Segmentation. , 2007, , .		47
43	A Localized Approach to Abandoned Luggage Detection with Foreground-Mask Sampling. , 2008, , .		46
44	A novel low-power full-search block-matching motion-estimation design for H.263+. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 890-897.	5.6	45
45	Analysis and reduction of reference frames for motion estimation in MPEG-4 AVC/JVT/H.264. , 0, , .		45
46	Content-Aware Prediction Algorithm With Inter-View Mode Decision for Multiview Video Coding. IEEE Transactions on Multimedia, 2008, 10, 1553-1564.	5.2	44
47	Analysis and design of macroblock pipelining for H.264/AVC VLSI architecture. , 0, , .		42
48	Seizure prediction based on classification of EEG synchronization patterns with on-line retraining and post-processing scheme. , 2011, 2011, 7564-9.		40
49	Architecture Design of H.264/AVC Decoder with Hybrid Task Pipelining for High Definition Videos. , 0, , .		38
50	Efficient VLSI architectures of lifting-based discrete wavelet transform by systematic design method. , 0, , .		37
51	Generic RAM-based architecture for two-dimensional discrete wavelet transform with line-based method. , 0, , .		37
52	iVisual: An Intelligent Visual Sensor SoC With 2790 fps CMOS Image Sensor and 205 GOPS/W Vision Processor. IEEE Journal of Solid-State Circuits, 2009, 44, 127-135.	3.5	37
53	An H.264/AVC scalable extension and high profile HDTV 1080p encoder chip. , 2008, , .		36
54	Bandwidth optimized motion compensation hardware design for H.264/AVC HDTV decoder. , 2005, , .		35

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55	A real-time 1080p 2D-to-3D video conversion system. IEEE Transactions on Consumer Electronics, 2011, 57, 915-922.	3.0	35
56	IC design of an adaptive Viterbi decoder. IEEE Transactions on Consumer Electronics, 1996, 42, 52-62.	3.0	34
57	Low-delay and error-robust wireless video transmission for video communications. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 1049-1058.	5.6	34
58	Parallel embedded block coding architecture for JPEG 2000. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1086-1097.	5.6	34
59	Algorithm and Architecture Design of Power-Oriented H.264/AVC Baseline Profile Encoder for Portable Devices. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1118-1128.	5.6	34
60	High speed memory efficient EBCOT architecture for JPEG2000. , 0, , .		33
61	Partial-result-reuse architecture and its design technique for morphological operations with flat structuring elements. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1156-1169.	5.6	29
62	Analysis and architecture design of EBCOT for JPEG-2000. , 0, , .		28
63	2.8 to 67.2mW Low-Power and Power-Aware H.264 Encoder for Mobile Applications. , 2007, , .		28
64	A 52 mW Full HD 160-Degree Object Viewpoint Recognition SoC With Visual Vocabulary Processor for Wearable Vision Applications. IEEE Journal of Solid-State Circuits, 2012, 47, 797-809.	3.5	28
65	Dual-block-pipelined VLSI architecture of entropy coding for H.264/AVC baseline profile. , 0, , .		27
66	A 59.5mW scalable/multi-view video decoder chip for Quad/3D Full HDTV and video streaming applications. , 2010, , .		27
67	VLSI implementation of a selective median filter. IEEE Transactions on Consumer Electronics, 1996, 42, 33-42.	3.0	26
68	Joint Prediction Algorithm and Architecture for Stereo Video Hybrid Coding Systems. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 1324-1337.	5.6	26
69	An MPEG audio decoder chip. IEEE Transactions on Consumer Electronics, 1995, 41, 89-96.	3.0	25
70	VLSI Architecture for Forward Discrete Wavelet Transform Based on B-spline Factorization. Journal of Signal Processing Systems, 2005, 40, 343-353.	1.0	24
71	One-pass computation-aware motion estimation with adaptive search strategy. IEEE Transactions on Multimedia, 2006, 8, 698-706.	5.2	24
72	A 2D-to-3D conversion system using edge information. , 2010, , .		24

#	ARTICLE	IF	CITATIONS
73	A Low-power Low-voltage Direct Digital Frequency Synthesizer. , 0, , .		22
74	Hybrid motion/depth-oriented inpainting for virtual view synthesis in multiview applications. , 2010, , .		22
75	Performance analysis and architecture evaluation of MPEG-4 video codec system. , 0, , .		21
76	Single Reference Frame Multiple Current Macroblocks Scheme for Multiple Reference Frame Motion Estimation in H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 242-247.	5.6	21
77	On-line empirical mode decomposition biomedical microprocessor for Hilbert Huang transform. , 2011, , .		21
78	Real-Time Depth Image based Rendering Hardware Accelerator for Advanced Three Dimensional Television System. , 2006, , .		20
79	On-Chip Memory Optimization Scheme for VLSI Implementation of Line-Based Two-Dimensional Discrete Wavelet Transform. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 814-822.	5.6	20
80	Fast motion estimation with inter-view motion vector prediction for stereo and multiview video coding. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	20
81	A block-based 2D-to-3D conversion system with bilateral filter. , 2009, , .		20
82	Visual Vocabulary Processor Based on Binary Tree Architecture for Real-Time Object Recognition in Full-HD Resolution. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2329-2332.	2.1	19
83	Computation reduction technique for lossy JPEG2000 encoding through EBCOT Tier-2 feedback processing. , 0, , .		18
84	Predictive line search: an efficient motion estimation algorithm for MPEG-4 encoding systems on multimedia processors. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 111-117.	5.6	18
85	Architecture design of full HD JPEG XR encoder for digital photography applications. IEEE Transactions on Consumer Electronics, 2008, 54, 963-971.	3.0	18
86	Single-iteration full-search fractional motion estimation for quad full HD H.264/AVC encoding. , 2009, , .		17
87	Localized Detection of Abandoned Luggage. Eurasip Journal on Advances in Signal Processing, 2010, , .	1.0	17
88	Reconfigurable Morphological Image Processing Accelerator for Video Object Segmentation. Journal of Signal Processing Systems, 2011, 62, 77-96.	1.4	17
89	Low Power Cache Algorithm and Architecture Design for Fast Motion Estimation in H.264/AVC Encoder System. , 2007, , .		16
90	Architecture design of high performance embedded compression for high definition video coding. , 2008, , .		16

#	ARTICLE	IF	CITATIONS
91	128-channel spike sorting processor with a parallel-folding structure in 90nm process. , 2009, , .		16
92	A branch selection multi-symbol high throughput CABAC decoder architecture for H.264/AVC. , 2009, , .		16
93	Vector quantization using tree-structured self-organizing feature maps. IEEE Journal on Selected Areas in Communications, 1994, 12, 1594-1599.	9.7	15
94	A high quality MC-OBTC Codec for video signal processing. IEEE Transactions on Circuits and Systems for Video Technology, 1994, 4, 92-98.	5.6	15
95	Rate-optimal DSP synthesis by pipeline and minimum unfolding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1994, 2, 81-88.	2.1	15
96	Performance analysis of hardware oriented algorithm modification in H.264. , 2003, , .		15
97	Memory analysis and architecture for two-dimensional discrete wavelet transform. , 0, , .		15
98	iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor. , 2008, , .		15
99	Cache-based integer motion/disparity estimation for quad-HD H.264/AVC and HD multiview video coding. , 2009, , .		15
100	Video stabilization for vehicular applications using SURF-like descriptor and KD-tree. , 2010, , .		15
101	Channel selection for epilepsy seizure prediction method based on machine learning. , 2012, 2012, 5162-5.		15
102	Analysis of EBCOT decoding algorithm and its VLSI implementation for JPEG 2000. , 0, , .		14
103	An efficient and low power architecture design for motion estimation using global elimination algorithm. , 2002, , .		14
104	Hardware architecture design for H.264/AVC intra frame coder. , 0, , .		14
105	Reconfigurable Discrete Wavelet Transform Processor for Heterogeneous Reconfigurable Multimedia Systems. Journal of Signal Processing Systems, 2005, 41, 35-47.	1.0	14
106	Relative Depth Layer Extraction for Monoscopic Video by Use of Multidimensional Filter. , 2006, , .		14
107	Hardware-efficient belief propagation. , 2009, , .		14
108	A multimedia semantic analysis SoC (SASoC) with machine-learning engine. , 2010, , .		14

#	ARTICLE	IF	CITATIONS
109	A flexible fully hardwired CABAC encoder for UHDTV H.264/AVC high profile video. IEEE Transactions on Consumer Electronics, 2012, 58, 1329-1337.	3.0	14
110	ASG: Automatic schematic generator. The Integration VLSI Journal, 1991, 11, 11-27.	1.3	13
111	A digital signal processor with programmable correlator array architecture for third generation wireless communication system. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 1110-1120.	2.3	13
112	Error concealment algorithm using interested direction for JPEG 2000 image transmission. IEEE Transactions on Consumer Electronics, 2003, 49, 1395-1401.	3.0	13
113	High performance two-symbol arithmetic encoder in JPEG 2000. , 0, , .		13
114	Multi-mode embedded compression codec engine for power-aware video coding system. , 0, , .		13
115	Low Power Entropy Coding Hardware Design for H.264/AVC Baseline Profile Encoder. , 2006, , .		13
116	Extended intelligent edge-based line average with its implementation and test method. , 0, , .		12
117	A multimedia video conference system: using region base hybrid coding. IEEE Transactions on Consumer Electronics, 1996, 42, 781-786.	3.0	12
118	A VLSI architecture design of VLC encoder for high data rate video/image coding. , 0, , .		12
119	Efficient video segmentation algorithm for real-time MPEG-4 camera system. , 2000, , .		12
120	Analysis and architecture design of lifting based DWT and EBCOT for JPEG 2000. , 0, , .		12
121	A Programmable Parallel VLSI Architecture for 2-D Discrete Wavelet Transform. Journal of Signal Processing Systems, 2001, 28, 151-163.	1.0	12
122	A novel hybrid motion estimator supporting diamond search and fast full search. , 0, , .		12
123	Low-power parallel tree architecture for full search block-matching motion estimation. , 0, , .		12
124	Bandwidth-efficient cache-based motion compensation architecture with DRAM-friendly data access control. , 2009, , .		12
125	Low power full-search block-matching motion estimation chip for H.263+. , 0, , .		11
126	A Low Power 8 x 8 Direct 2-D DCT Chip Design. Journal of Signal Processing Systems, 2000, 26, 319-332.	1.0	11

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127	Four field local motion compensated de-interlacing. , 0, , .		11
128	Novel precompression rate-distortion optimization algorithm for JPEG 2000. , 2004, , .		11
129	Stereo Video Coding System with Hybrid Coding Based on Joint Prediction Scheme. , 0, , .		11
130	Precompression Quality-Control Algorithm for JPEG 2000. IEEE Transactions on Image Processing, 2006, 15, 3279-3293.	6.0	11
131	System Analysis of VLSI Architecture for 5/3 and 1/3 Motion-Compensated Temporal Filtering. IEEE Transactions on Signal Processing, 2006, 54, 4004-4014.	3.2	11
132	Algorithm analysis and architecture design for HDTV applications. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2006, 22, 22-31.	0.8	11
133	Low power and power aware fractional motion estimation of H.264/AVC for mobile applications. , 0, , .		11
134	VLSI Architecture Design of Fractional Motion Estimation for H.264/AVC. Journal of Signal Processing Systems, 2008, 53, 335-347.	1.4	11
135	Priority depth fusion for the 2D to 3D conversion system. Proceedings of SPIE, 2008, , .	0.8	11
136	Pyramid Architecture for 3840 X 2160 Quad Full High Definition 30 Frames/s Video Acquisition. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1499-1508.	5.6	11
137	Accurate and Bandwidth Efficient Architecture for CNN-based Full-HD Super-Resolution. , 2018, , .		11
138	A real-time video signal processing chip. IEEE Transactions on Consumer Electronics, 1993, 39, 82-92.	3.0	10
139	A programmable VLSI architecture for 2-D discrete wavelet transform. , 0, , .		10
140	Bit-plane error recovery via cross subband for image transmission in JPEG2000. , 0, , .		10
141	Multi-Mode Content-Aware Motion Estimation Algorithm for Power-Aware Video Coding Systems. , 0, , .		10
142	Single Reference Frame Multiple Current Macroblocks Scheme for Multi-Frame Motion Estimation in H.264/AVC. , 0, , .		10
143	Hardware architecture design of an H.264/AVC video codec. , 0, , .		10
144	Architecture Design of Area-Efficient SRAM-Based Multi-Symbol Arithmetic Encoder in H.264/AVC. , 0, , .		10

#	ARTICLE	IF	CITATIONS
145	Single iteration view interpolation for multiview video applications. , 2009, , .		10
146	Architecture design of stereo matching using belief propagation. , 2010, , .		10
147	A 69mW 140-meter/60fps and 60-meter/300fps intelligent vision SoC for versatile automotive applications. , 2012, , .		10
148	An intelligent depth-based obstacle detection system for visually-impaired aid applications. , 2012, , .		10
149	23.2 A 1920×1080 30fps 611 mW five-view depth-estimation processor for light-field applications. , 2015, , .		10
150	Concurrent error-detectable butterfly chip for real-time FFT processing through time redundancy. IEEE Journal of Solid-State Circuits, 1993, 28, 537-547.	3.5	9
151	A 32-bit logarithmic number system processor. Journal of Signal Processing Systems, 1996, 14, 311-319.	1.0	9
152	A novel MPEG-2 audio decoder with efficient data arrangement and memory configuration. IEEE Transactions on Consumer Electronics, 1997, 43, 598-604.	3.0	9
153	Scalable module-based architecture for MPEG-4 BMA motion estimation. , 0, , .		9
154	Design and implementation of a bitstream parsing coprocessor for MPEG-4 video system-on-chip solution. , 0, , .		9
155	VLSI implementation of shape-adaptive discrete wavelet transform. , 2002, , .		9
156	VLSI architecture design of MPEG-4 shape coding. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 741-751.	5.6	9
157	iVisual. , 2008, , .		9
158	51.3: An Ultra-Low-Cost 2-D/3-D Video-Conversion System. Digest of Technical Papers SID International Symposium, 2010, 41, 766.	0.1	9
159	Feature-based video stabilization for vehicular applications. , 2010, , .		9
160	An intelligent vision-based vehicle detection and tracking system for automotive applications. , 2011, , .		9
161	Efficient Hardware Architecture for Large Disparity Range Stereo Matching Based on Belief Propagation. , 2016, , .		9
162	A low power 2D DCT chip design using direct 2D algorithm. , 0, , .		8

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163	Flipping structure: an efficient VLSI architecture for lifting-based discrete wavelet transform. , 0, , .		8
164	Motion adaptive de-interlacing by horizontal motion detection and enhanced ELA processing. , 0, , .		8
165	An Efficient Embedded Bitstream Parsing Processor for MPEG-4 Video Decoding System. Journal of Signal Processing Systems, 2005, 41, 183-191.	1.0	8
166	Memory Analysis of VLSI Architecture for 5/3 and 1/3 Motion-Compensated Temporal Filtering. , 0, , .		8
167	Power-Scalable Algorithm and Reconfigurable Macro-Block Pipelining Architecture of H.264 Encoder for Mobile Application. , 2006, , .		8
168	High-performance JPEG 2000 encoder with rate-distortion optimization. IEEE Transactions on Multimedia, 2006, 8, 645-653.	5.2	8
169	System Bandwidth Analysis of Multiview Video Coding with Precedence Constraint. , 2007, , .		8
170	Computation-Free Motion Estimation with Inter-View Mode Decision for Multiview Video Coding. , 2007, , .		8
171	Data Reuse Exploration for Low Power Motion Estimation Architecture Design in H.264 Encoder. Journal of Signal Processing Systems, 2008, 50, 1-17.	1.4	8
172	Efficient Architecture Design of Motion-Compensated Temporal Filtering/Motion Compensated Prediction Engine. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 98-109.	5.6	8
173	Analysis of belief propagation for hardware realization. , 2008, , .		8
174	Fast belief propagation process element for high-quality stereo estimation. , 2009, , .		8
175	Hybrid depth cueing for 2D-to-3D conversion system. Proceedings of SPIE, 2009, , .	0.8	8
176	Multichannel evoked neural signal compression using advanced video compression algorithm. , 2009, , .		8
177	Accuracy and power tradeoff in spike sorting microsystems with cubic spline interpolation. , 2010, , .		8
178	Robust heart rate measurement with phonocardiogram by on-line template extraction and matching. , 2011, 2011, 1957-60.		8
179	A real-time system for object detection and location reminding with RGB-D camera. , 2014, , .		8
180	Fast realistic refocusing for sparse light fields. , 2015, , .		8

#	ARTICLE	IF	CITATIONS
181	A self-adjusting weighted median filter for removing impulse noise in images. , 0, , .		7
182	A novel image compression algorithm by using Log-Exp transform. , 0, , .		7
183	Design of a low power psycho-acoustic model co-processor for MPEG-2/4 AAC LC stereo encoder. , 0, , .		7
184	Power-efficient FIR filter architecture design for wireless embedded system. IEEE Transactions on Circuits and Systems II: Express Briefs, 2004, 51, 21-25.	2.2	7
185	A low complexity design of psycho-acoustic model for MPEG-2/4 advanced audio coding. IEEE Transactions on Consumer Electronics, 2004, 50, 1209-1217.	3.0	7
186	JPEG, MPEG-4, and H.264 Codec IP Development. , 0, , .		7
187	Memory Efficient JPEG 2000 Architecture with Stripe Pipeline Scheme. , 0, , .		7
188	Fast decomposition of filterbanks for the state-of-the-art audio coding. IEEE Signal Processing Letters, 2005, 12, 693-696.	2.1	7
189	Hardware oriented content-adaptive fast algorithm for variable block-size integer motion estimation in H.264. , 2005, , .		7
190	Novel Configurable Architecture of ML-Decomposed Binary Arithmetic Encoder for Multimedia Applications. , 2007, , .		7
191	A Quality-of-Experience Video Adaptor for Serving Scalable Video Applications. IEEE Transactions on Consumer Electronics, 2007, 53, 1130-1137.	3.0	7
192	Architecture Design of Fine Grain Quality Scalable Encoder with CABAC for H.264/AVC Scalable Extension. Journal of Signal Processing Systems, 2010, 60, 363-375.	1.4	7
193	Analysis and design of on-sensor ECG processors for realtime detection of VF, VT, and PVC. , 2010, , .		7
194	1.4µW/channel 16-channel EEG/ECoG processor for smart brain sensor SoC. , 2010, , .		7
195	Design and implementation of cubic spline interpolation for spike sorting microsystems. , 2011, , .		7
196	Brain-Inspired Framework for Fusion of Multiple Depth Cues. IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23, 1137-1149.	5.6	7
197	Object-oriented video coding algorithm for very low bit-rate system. , 0, , .		6
198	VLSI implementation of the motion estimator with two-dimensional data-reuse. IEEE Transactions on Consumer Electronics, 1998, 44, 623-629.	3.0	6

#	ARTICLE	IF	CITATIONS
199	Reconfigurable discrete wavelet transform architecture for advanced multimedia systems. , 0, , .		6
200	Motion compensated de-interlacing with adaptive global motion estimation and compensation. , 0, , .		6
201	Platform-based MPEG-4 video encoder SoC design. , 0, , .		6
202	Multiple-lifting Scheme: Memory-efficient VLSI Implementation for Line-based 2-D DWT. , 0, , .		6
203	Memory Efficient JPEG 2000 Architecture With Stripe Pipeline Scheduling. IEEE Transactions on Signal Processing, 2006, 54, 4807-4816.	3.2	6
204	Hybrid Morphology Processing Unit Architecture for Moving Object Segmentation Systems. Journal of Signal Processing Systems, 2006, 42, 241-255.	1.0	6
205	Bandwidth-Efficient Encoder Framework for H.264/AVC Scalable Extension. , 2007, , .		6
206	An 8.6mW 12.5Mvertices/s 800MOPS 8.91mm ² Stream Processor Core for Mobile Graphics and Video Applications. , 2007, , .		6
207	124 MSamples/s Pixel-Pipelined Motion-JPEG 2000 Codec Without Tile Memory. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 398-406.	5.6	6
208	Pipelined arithmetic encoder design for lossless JPEG XR encoder. , 2009, , .		6
209	An exploration of on-road vehicle detection using hierarchical scaling schemes. , 2010, , .		6
210	A real-time 1080p 2D-to-3D video conversion system. , 2011, , .		6
211	Cubic spline interpolation with overlapped window and data reuse for on-line Hilbert Huang transform biomedical microprocessor. , 2011, 2011, 7091-4.		6
212	Low power 2D DCT chip design for wireless multimedia terminals. , 0, , .		5
213	Design and analysis of VLSI-based arithmetic arrays with error correction. International Journal of Electronics, 1992, 72, 253-271.	0.9	5
214	A novel video signal processor with programmable data arrangement and efficient memory configuration. IEEE Transactions on Consumer Electronics, 1996, 42, 526-534.	3.0	5
215	Robust error concealment algorithm for MPEG-4 with the aid of fuzzy theory. , 0, , .		5
216	Partial-result-reuse architecture and its design technique for morphological operations. , 0, , .		5

#	ARTICLE	IF	CITATIONS
217	Single chip video segmentation system with a programmable PE array. , 0, , .		5
218	Predictive watershed for image sequences segmentation. , 2002, , .		5
219	Simple and effective algorithm for automatic tracking of a single object using a pan-tilt-zoom camera. , 0, , .		5
220	Platform architecture design for MPEG-4 video coding. , 0, , .		5
221	<title>Fast motion estimation algorithm for H.264/MPEG-4 AVC by using multiple reference frame skipping criteria</title>. , 2003, , .		5
222	Reconfigurable discrete cosine transform processor for object-based video signal processing. , 0, , .		5
223	One-Pass Computation-Aware Motion Estimation with Adaptive Search Strategy. , 0, , .		5
224	Analysis and Hardware Architecture Design of Global Motion Estimation. Journal of Signal Processing Systems, 2008, 53, 285-300.	1.4	5
225	Frame-parallel design strategy for high definition B-frame H.264/AVC encoder. , 2008, , .		5
226	Algorithm and architecture design of cache system for motion estimation in high definition H.264/AVC. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	5
227	Algorithm and architecture for object tracking using particle filter. , 2009, , .		5
228	A 216fps 4096×2160p 3DTV set-top box SoC for free-viewpoint 3DTV applications. , 2011, , .		5
229	A 172.6mW 43.8GFLOPS energy-efficient scalable eight-core 3D graphics processor for mobile multimedia applications. , 2011, , .		5
230	Analysis and Design of On-sensor ECG Processors for Realtime Detection of Cardiac Anomalies Including VF, VT, and PVC. Journal of Signal Processing Systems, 2011, 65, 275-285.	1.4	5
231	Low power and high accuracy spike sorting microprocessor with on-line interpolation and re-alignment in 90nm CMOS process. , 2012, 2012, 4485-8.		5
232	A 1.0TOPS/W 36-core neocortical computing processor with 2.3Tb/s Kautz NoC for universal visual recognition. , 2012, , .		5
233	A 130.3mW 16-core mobile GPU with power-aware approximation techniques. , 2013, , .		5
234	A 130.3 mW 16-Core Mobile GPU With Power-Aware Pixel Approximation Techniques. IEEE Journal of Solid-State Circuits, 2015, 50, 2212-2223.	3.5	5

#	ARTICLE	IF	CITATIONS
235	Efficient stereo video coding system for immersive teleconference with two-stage hybrid disparity estimation algorithm. , 0, , .		4
236	A single-chip Viterbi decoder for a binary convolutional code using an adaptive algorithm. IEEE Transactions on Consumer Electronics, 1995, 41, 150-159.	3.0	4
237	A bit-level pipelined VLSI architecture for the running order algorithm. IEEE Transactions on Signal Processing, 1997, 45, 2140-2144.	3.2	4
238	Efficient algorithms and architectures for MPEG-4 object-based video coding. , 0, , .		4
239	Automatic threshold decision of background registration technique for video segmentation. , 2002, , .		4
240	A new error concealment algorithm for H.264 video transmission. , 0, , .		4
241	Area efficient architecture for the embedded block coding in JPEG 2000. , 0, , .		4
242	System analysis of VLSI architecture for motion-compensated temporal filtering. , 2005, , .		4
243	Four Field Variable Block Size Motion Compensated Adaptive De-interlacing. , 0, , .		4
244	Algorithm and architecture optimization for full-mode encoding of H.264/AVC intra prediction. , 2005, , .		4
245	Line Buffer Wordlength Analysis for Line-Based 2-D DWT. , 0, , .		4
246	Design and Implementation Of Word-Level Embedded Block Coding Architecture in JPEG 2000 Decoder. , 0, , .		4
247	124Ms/s pixel-pipelined motion-JPEG 2000 codec without tile memory. , 2006, , .		4
248	Low Power Programmable Shader with Efficient Graphics And Video Acceleration Capabilities for Mobile Multimedia Applications. , 0, , .		4
249	A 100 MHz 1920x1080 HD-Photo 20 frames/sec JPEG XR encoder design. , 2008, , .		4
250	11.4: A Quality-Aware Scalable Depth-Aware Video Processing System. Digest of Technical Papers SID International Symposium, 2009, 40, 123-126.	0.1	4
251	Learning-Based Vehicle Detection Using Up-Scaling Schemes and Predictive Frame Pipeline Structures. , 2010, , .		4
252	Low-cost hardware architecture design for 3D warping engine in multiview video applications. , 2010, , .		4

#	ARTICLE	IF	CITATIONS
253	Sub-microwatt correlation integral processor for implantable closed-loop epileptic neuromodulator. , 2010, , .		4
254	Tera-Scale Performance Machine Learning SoC (MLSoC) With Dual Stream Processor Architecture for Multimedia Content Analysis. IEEE Journal of Solid-State Circuits, 2010, , .	3.5	4
255	Video encoder design for high-definition 3D video communication systems. , 2010, 48, 76-86.		4
256	ReSSP: A 5.877 TOPS/W Reconfigurable Smart-camera Stream Processor. , 2011, , .		4
257	An intelligent depth-based obstacle detection for mobile applications. , 2012, , .		4
258	On-the-fly fashion photograph recommendation system with robust face shape features. , 2014, , .		4
259	Design and implementation of a low power spike detection processor for 128-channel spike sorting microsystem. , 2014, , .		4
260	A flexible high-throughput VLSI architecture with 2-D data-reuse for full-search motion estimation. , 0, , .		3
261	A LOG-EXP still image compression chip design. IEEE Transactions on Consumer Electronics, 1999, 45, 812-819.	3.0	3
262	Computationally controllable integer, half, and quarter-pel motion estimator for MPEG-4 Advanced Simple Profile. , 0, , .		3
263	VLSI Architecture for Lifting-Based Shape-Adaptive Discrete Wavelet Transform with Odd-Symmetric Filters. Journal of Signal Processing Systems, 2005, 40, 175-188.	1.0	3
264	Analysis and architecture for memory efficient JBIG2 arithmetic encoder. , 2005, , .		3
265	Nearly Lossless Content-Dependent Low-Power DCT Design for Mobile Video Applications. , 0, , .		3
266	Architecture Design of Fine Grain SNR Scalable Encoder with CABAC for H.264/AVC Scalable Extension. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	3
267	System Architecture Design Methodology for H.264/AVC Encoder. , 2007, , .		3
268	A 212MPixels/s 4096×2160p multiview video encoder chip for 3D/quad HDTV applications. , 2009, , .		3
269	On-chip principal component analysis with a mean pre-estimation method for spike sorting. , 2009, , .		3
270	Video 2-3-conversion based on hybrid depth cueing. Journal of the Society for Information Display, 2010, 18, 704-716.	0.8	3

#	ARTICLE	IF	CITATIONS
271	A cortex-like model for rapid object recognition using feature-selective hashing. , 2011, , .		3
272	Trends in Design and Implementation of Signal Processing Systems [In the Spotlight]. IEEE Signal Processing Magazine, 2011, 28, 192-193.	4.6	3
273	Algorithm and implementation of multi-channel spike sorting using GPU in a home-care surveillance system. , 2011, , .		3
274	Robust moving object tracking and trajectory prediction for visual navigation in dynamic environments. , 2012, , .		3
275	A Chip Architecture for Compressive Sensing Based Detection of IC Trojans. , 2012, , .		3
276	Automatic video segmentation and object tracking with real-time RGB-D data. , 2014, , .		3
277	Interactive clothing retrieval system. , 2014, , .		3
278	Intelligent Content-Aware Model-Free Low Power Evoked Neural Signal Compression. Lecture Notes in Computer Science, 2008, , 898-901.	1.0	3
279	Pipeline interleaving design for FIR, IIR, and FFT array processors. Journal of Signal Processing Systems, 1995, 10, 275-293.	1.0	2
280	Scalable implementation scheme for multirate FIR filters and its application in efficient design of subband filter banks. IEEE Transactions on Circuits and Systems for Video Technology, 1996, 6, 407-410.	5.6	2
281	An efficient visual pattern block truncation coding. , 0, , .		2
282	Error resilience for block loss with overlapped motion compensation. , 0, , .		2
283	A block shifting method for reduction of blocking effects in subband/wavelet image coding. IEEE Transactions on Consumer Electronics, 1998, 44, 170-177.	3.0	2
284	Using a region-based blurring method and bits reallocation to enhance quality on face region in very low bitrate video. , 0, , .		2
285	Low power strategy about correlator array for CDMA baseband processor. , 0, , .		2
286	IP design of a reconfigurable baseline JPEG coding. , 0, , .		2
287	MPEG-4 video bitstream structure analysis and its parsing architecture design. , 0, , .		2
288	Automatic video segmentation for MPEG-4 using predictive watershed. , 2001, , .		2

#	ARTICLE	IF	CITATIONS
289	Analysis and architecture design of JPEG2000. , 2001, , .		2
290	A hybrid morphology processing units architecture for real-time video segmentation systems. , 0, , .		2
291	Hardware-efficient architecture design of tree-depth scanning and multiple quantization scheme for MPEG-4 still texture coding. , 0, , .		2
292	Multiple sprites and frame skipping techniques for sprite generation with high subjective quality and fast speed. , 0, , .		2
293	A hardware accelerator for video segmentation using programmable morphology PE array. , 0, , .		2
294	Algorithm and architecture of video segmentation hardware system with a programmable PE array. , 0, , .		2
295	An efficient embedded bitstream parsing processor for MPEG-4 video decoding system. , 0, , .		2
296	VLSI architecture for discrete wavelet transform based on B-spline factorization. , 0, , .		2
297	Novel word-level algorithm of embedded block coding in JPEG 2000. , 2003, , .		2
298	Parallel global elimination algorithm and architecture design for fast block matching motion estimation. , 0, , .		2
299	Hybrid-mode embedded compression for H.264/AVC video coding system. , 2005, , .		2
300	Algorithm and architecture of prediction core in stereo video hybrid coding system. , 0, , .		2
301	Frame-level data reuse for motion-compensated temporal filtering. , 0, , .		2
302	Analysis of scalable architecture for the embedded block coding in JPEG 2000. , 0, , .		2
303	Adaptive Tile Depth Filter for the Depth Buffer Bandwidth Minimization in the Low Power Graphics Systems. , 0, , .		2
304	Word-Level Parallel Architecture of JPEG 2000 Embedded Block Coding Decoder. IEEE Transactions on Multimedia, 2007, 9, 1103-1112.	5.2	2
305	A 26mW 6.4GFLOPS multi-core stream processor for mobile multimedia applications. , 2008, , .		2
306	Bio-inspired unified model of visual segmentation system for CAPTCHA character recognition. , 2008, , .		2

#	ARTICLE	IF	CITATIONS
307	Mapping Scalable Video Coding decoder on multi-core stream processors. , 2009, , .		2
308	Low bandwidth decoder framework for H.264/AVC scalable extension. , 2010, , .		2
309	Smart display: A mobile self-adaptive projector-camera system. , 2011, , .		2
310	Architecture design of the multi-functional wavelet-based ECG microprocessor for realtime detection of abnormal cardiac events. , 2012, 2012, 4466-9.		2
311	A viewer centric depth adjustment for stereoscopic images. , 2012, , .		2
312	Low-power multi-processor system architecture design for universal biomedical signal processing. , 2013, , .		2
313	3D hand localization by low-cost webcams. Proceedings of SPIE, 2013, , .	0.8	2
314	An integrated system for object tracking, detection, and online learning with real-time RGB-D video. , 2014, , .		2
315	Memory efficient architecture for belief propagation based disparity estimation. , 2015, , .		2
316	Accurate and fast segment-based cost aggregation algorithm for stereo matching. , 2017, , .		2
317	Building a pseudo object-oriented very low bit-rate video coding system from a modified optical flow motion estimation algorithm. , 0, , .		2
318	Rate-optimal static scheduling for recursive DSP algorithms by retiming and unfolding. International Journal of Electronics, 1992, 73, 687-701.	0.9	1
319	Rate-Optimal DSP Synthesis by Pipeline and Minimum Unfolding. , 0, , .		1
320	Investigation of a visual telephone prototyping on personal computers. IEEE Transactions on Consumer Electronics, 1996, 42, 750-759.	3.0	1
321	A very low bit rate video coding system using adaptive region-classified vector quantization. , 0, , .		1
322	An efficient array architecture with data-rings for 3-step hierarchical search block matching algorithm. , 0, , .		1
323	<title>Architecture design of motion estimation for ITU-T H.263</title>. , 1997, 3024, 482.		1
324	A flexible data-interlacing architecture for full-search block-matching algorithm. , 0, , .		1

#	ARTICLE	IF	CITATIONS
325	An I-phone system design and implementation with a portable speech coding coprocessor. IEEE Transactions on Consumer Electronics, 1997, 43, 1262-1269.	3.0	1
326	VLSI implementation of visual block pattern truncation coding. IEEE Transactions on Consumer Electronics, 1998, 44, 490-499.	3.0	1
327	A single chip CMOS APS camera with direct frame difference output. , 0, , .		1
328	<title>Efficient architecture of binary motion estimation for MPEG-4 shape coding</title>. , 2000, , .		1
329	A novel architecture of inverse quantization and multichannel processing for MPEG-2 audio decoding. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 75-78.	2.3	1
330	Embedded JPEG encoder IP core and memory efficient preprocessing architecture for scanner. , 0, , .		1
331	CDSP: an application-specific digital signal processor for third generation wireless communications. IEEE Transactions on Consumer Electronics, 2001, 47, 672-677.	3.0	1
332	A real-time practical video segmentation algorithm for MPEG-4 camera systems. , 0, , .		1
333	Hardware implementation of shape-adaptive discrete wavelet transform with the JPEG2000 defaulted (9,7) filter bank. , 0, , .		1
334	Performance analysis of hardware oriented algorithm modifications in H.264. , 0, , .		1
335	Perspectives of multimedia SoC. , 0, , .		1
336	Unsupervised object-based sprite coding system for tennis sport. , 2003, , .		1
337	Analysis and reduction of reference frames for motion estimation in MPEG-4 AVC/JVT/H.264. , 2003, , .		1
338	<title>Fast disparity estimation algorithm for mesh-based stereo image/video compression with two-stage hybrid approach</title>. , 2003, , .		1
339	LSI design for MPEG-4 coding system. , 0, , .		1
340	MPEG-4 FGS encoder design for an interactive content-aware MPEG-4 video streaming SOC. , 0, , .		1
341	Architecture and analysis of color structure and scalable color descriptor for real-time video indexing and retrieval. , 0, , .		1
342	Hardware architecture for global motion estimation for MPEG-4 Advanced Simple Profile. , 0, , .		1

#	ARTICLE	IF	CITATIONS
343	Memory and Computationally Efficient Psychoacoustic Model for MPEG AAC on 16-bit Fixed-point Processors. , 0, , .		1
344	Application Layer Error Correction Scheme for Video Header Protection on Wireless Network. , 0, , .		1
345	Design and Implementation of JPEG 2000 Codec with Bit-Plane Scalable Architecture. , 2006, , .		1
346	Platform-Based MPEG-4 SOC Design for Video Communications. Journal of Signal Processing Systems, 2006, 42, 7-19.	1.0	1
347	Architecture Design of Low Power Integer Motion Estimation for H. 264/AVC. , 0, , .		1
348	Spatial-temporal consistent labeling for multi-camera multi-object surveillance systems. , 2008, , .		1
349	Optimal Transform of Multichannel Evoked Neural Signals Using a Video Compression Algorithm. , 2009, , .		1
350	Tera-scale performance machine learning SoC with dual stream processor architecture for multimedia content analysis. , 2009, , .		1
351	Plenary presentation B. , 2009, , .		1
352	Efficient message reduction algorithm for stereo matching using belief propagation. , 2010, , .		1
353	Perceptual multi-cues 2D-to-3D conversion system. , 2011, , .		1
354	Assessing normality of heart sound by matching pursuit residue with frequency-domain-based templates. , 2012, 2012, 2917-20.		1
355	WarmL1: A warm-start homotopy-based reconstruction algorithm for sparse signals. , 2012, , .		1
356	Accurate positioning system based on street view recognition. , 2012, , .		1
357	CRISP-II: Coarse-grained reconfigurable image stream processor for image-processing and intelligent operations in QFHD video cameras. , 2012, , .		1
358	Acquire user's distance by face detection. , 2013, , .		1
359	Evolving technology integration for consumer electronics. , 2013, , .		1
360	Video Stereo Matching with Temporally Consistent Belief Propagation. , 2018, , .		1

#	ARTICLE	IF	CITATIONS
361	A 473 μ W wireless 16-channel neural recording SoC with RF energy harvester. , 2018, , .		1
362	Hardware- and Memory-Efficient Architecture for Disparity Estimation of Large Label Counts. IEEE Transactions on Circuits and Systems for Video Technology, 2021, 31, 3679-3693.	5.6	1
363	Multimedia IP Development. , 2006, , 19-72.		1
364	Efficient hierarchical motion estimation algorithm based on visual pattern block segmentation. , 0, , .		1
365	The radix-2/sup k/ Viterbi decoding with transpose path metric processor. , 0, , .		0
366	Design and VLSI implementation of MPEG audio decoder. , 0, , .		0
367	VLSI-based array dividers with concurrent error detection. International Journal of Electronics, 1995, 78, 1139-1148.	0.9	0
368	Scalable implementation scheme for multirate FIR filters and its application in efficient design of subband filter banks. , 0, , .		0
369	A hardware-oriented design for weighted median filters. , 0, , .		0
370	A new design and implementation of 8 \times 8 2-D DCT/IDCT. , 0, , .		0
371	Design strategy for three-dimensional subband filter banks. , 0, , .		0
372	A Novel MPEG-2 Audio Decoder With Efficient Data Arrangement And Memory Configuration. , 1997, , .		0
373	A True Color Video Signal Processing System And Its Real-time Chip Implementation. , 1997, , .		0
374	Hardware efficient design of filter banks for video coding. , 0, , .		0
375	The system implementation of I-phone hardware by using low bit rate speech coding. , 0, , .		0
376	Jointly Optimal Region-Classified Adaptive Vector Quantization for Very Low Bit Rate Video Coding. Journal of Signal Processing Systems, 1997, 17, 189-200.	1.0	0
377	Vlsi Implementation Of Visual Block Pattern Truncation Coding. , 1998, , .		0
378	A simple and low-cost MPEG audio degrouping algorithm. , 0, , .		0

#	ARTICLE	IF	CITATIONS
379	Vlsi Implementation Of The Motion Estimator With Two-dimensional Data-reuse. , 1998, , .		0
380	A modified MPEG-2 audio decoding scheme based on its low-cost fast algorithm and efficient data scheduling. , 0, , .		0
381	A low-cost architecture design with efficient data arrangement and memory configuration for MPEG-2 audio decoder. , 0, , .		0
382	A cost effective architecture design of inverse quantization and multichannel processing for MPEG-2 audio decoding. , 0, , .		0
383	A cost-effective design for MPEG2 audio decoder with embedded RISC core. , 0, , .		0
384	Design and implementation of JPEG encoder IP core. , 0, , .		0
385	CDSP: an application-specific digital signal processor for third generation wireless communications. , 0, , .		0
386	Error-propagation analysis and concealment strategy for MPEG-4 video bitstream with data partitioning. , 2001, , .		0
387	A Cost-Effective Design for MPEG-2 Audio Decoder with Embedded RISC Core. Journal of Signal Processing Systems, 2001, 29, 255-265.	1.0	0
388	An efficient linear-phase FIR filter architecture design for wireless embedded system. , 0, , .		0
389	Low delay, error robust wireless video transmission architecture for video communication. , 0, , .		0
390	An efficient architecture for two-dimensional inverse discrete wavelet transform. , 0, , .		0
391	Error concealment algorithm using interested direction for JPEG 2000 image transmission. , 0, , .		0
392	Hardware oriented rate control algorithm and implementation for realtime video coding. , 2003, , .		0
393	Hardware-oriented optimization and block-level architecture design for MPEG-4 FGS encoder. , 0, , .		0
394	Hardware oriented rate control algorithm and implementation for realtime video coding. , 0, , .		0
395	B-spline factorization-based architecture for inverse discrete wavelet transform. , 0, , .		0
396	Hardware architecture design for visual processing: present and future. , 0, , .		0

#	ARTICLE	IF	CITATIONS
397	Architecture of MPEG-7 color structure description generator for realtime video applications. , 0, , .		0
398	Architecture of Global Motion Compensation for MPEG-4 Advanced Simple Profile. , 0, , .		0
399	Area Efficient Architecture for the Embedded Block Coding in JPEG 2000. , 2005, , .		0
400	Reconfigurable Platform for Content Science Research. , 0, , .		0
401	720 Å– 480 30fps Efficient Prediction Core Chip for Stereo Video Hybrid Coding System. , 2005, , .		0
402	Scalable Rate-Distortion-Computation Hardware Accelerator for MCTF and ME. , 2006, , .		0
403	Algorithm and Hardware Architecture Design for Weighted Prediction in H.264/MPEG-4 AVC. , 0, , .		0
404	Interactive Content-aware Video Streaming System with Fine Granularity Scalability. Journal of Signal Processing Systems, 2006, 44, 117-134.	1.0	0
405	Analysis and VLSI architecture of update step in motion-compensated temporal filtering. , 0, , .		0
406	Reconfigurable architecture for video applications. , 2007, , .		0
407	3D Video Applications and Intelligent Video Surveillance Camera and its VLSI Design. , 2007, , .		0
408	Multiview video hybrid coding system with texture-depth synthesis. , 2008, , .		0
409	A cost effective reconfigurable memory for multimedia multithreading streaming architecture. , 2008, , .		0
410	A real-time augmented view synthesis system for transparent car pillars. , 2008, , .		0
411	Intelligent image inpainting based on a brain-mimicking Recognition-Mining-Synthesis network. , 2009, , .		0
412	Tera-scale performance image stream processor with SoC architecture for multimedia content analysis. , 2009, , .		0
413	A 0.077 to 0.168 nJ/bit/iteration scalable 3GPP LTE turbo decoder with an adaptive sub-block parallel scheme and an embedded DVFS engine. , 2010, , .		0
414	A novel hybrid pipeline design methodology on a multi-cores streaming system for multimedia applications. , 2010, , .		0

#	ARTICLE	IF	CITATIONS
415	Hybrid color compensation for virtual view synthesis in multiview video applications. , 2010, , .		0
416	System scheduling analysis for high definition multiview video encoder. , 2010, , .		0
417	Intelligent 3D online virtual conferencing system with natural human-computer interaction. , 2011, , .		0
418	P-45: A Quality Measurement Based on Object Formation for 3D Contents. Digest of Technical Papers SID International Symposium, 2011, 42, 1265-1268.	0.1	0
419	Mobile energy expenditure tracking system based on heart rate and motion providing extra extensions for personalized care. , 2011, 2011, 5256-9.		0
420	Power estimation scheme for lowpower oriented biomedical SoC extended to very deep submicron technology. , 2011, , .		0
421	Six-dimensional free-viewpoint synthesis flow for QFHD free-viewpoint/multiview 3DTV applications. , 2011, , .		0
422	Density-based hardware-oriented classification for spike sorting microsystems. , 2011, , .		0
423	Algorithm and architecture design of a knowledge-based vehicle tracking for intelligent cruise control. , 2011, , .		0
424	A high speed feature matching architecture for real-time video stabilization. , 2012, , .		0
425	iSense3D: A real-time viewpoint-aware 3D video synthesis system. , 2012, , .		0
426	Compressive Sensing based Client-Cloud system for 3D depth reconstruction. , 2012, , .		0
427	3D image correction by Hilbert Huang decomposition. , 2012, , .		0
428	Exploration of reusing the pre-recorded training data set to improve the supervised classifier for EEG-based motor-imagery brain computer interfaces. , 2012, , .		0
429	A depth adaptation system based on perceptual horopter effect. , 2012, , .		0
430	Fast adaptive loop filter algorithm for high efficiency video coding. , 2012, , .		0
431	A real-time multi-user face unlock system via fast sparse coding approximation. , 2012, , .		0
432	Intelligent document capturing and blending system based on robust feature matching with an active camera. , 2013, , .		0

#	ARTICLE	IF	CITATIONS
433	Guest Editorial: Special Section on New Software/Hardware Paradigms for Error-Tolerant Multimedia Systems. IEEE Transactions on Multimedia, 2013, 15, 241-241.	5.2	0
434	Region-of-unpredictable determination for accelerated full-frame feature generation in video sequences. , 2014, , .		0
435	A spatial first 3-D XYT feature point extraction algorithm for efficient human action recognition. , 2014, , .		0
436	A real-time 3D interactive system with stereo camera in the uncertain background. , 2015, , .		0
437	Incremental new actions learning system with limited cost and storage. , 2015, , .		0
438	A 120 fps 1080p resolution block-based feature extraction architecture implementation for real-time action recognition. , 2017, , .		0
439	A Computational Efficient Architecture for Extremely Sparse Stereo Network. , 2021, , .		0
440	CMWMF: Constant Memory Architecture of Weighted Mode/Median Filter for Extremely Large Label Depth Refinement. IEEE Transactions on Circuits and Systems for Video Technology, 2021, 31, 2981-2993.	5.6	0
441	Dances with multimedia. , 2006, , .		0
442	H.264/AVC Video Codec Design A Hardwired Approach. Internet and Communications, 2008, , 169-212.	0.2	0
443	Video Compression. , 2010, , 103-121.		0
444	A novel video signal processor with reconfigurable pipelined architecture. , 0, , .		0
445	Hardware-efficient belief propagation. , 2009, , .		0
446	An adaptive network control scheme for region-based hybrid coding algorithm. , 0, , .		0
447	Bandwidth-Efficient Encoder Framework for H.264/AVC Scalable Extension. , 2007, , .		0