Liang-Gee Chen

List of Publications by Year
in descending order

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447 papers	7,042 citations	101543 36 h-index	114465 63 g-index
449 all docs	449 docs citations	449 times ranked	2312 citing authors

#	Article	IF	Citations
1	Efficient moving object segmentation algorithm using background registration technique. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 577-586.	8.3	293
2	Analysis and architecture design of an HDTV720p 30 frames/s H.264/AVC encoder. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 673-688.	8.3	251
3	Analysis, fast algorithm, and VLSI architecture design for H.264/AVC intra frame coder. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 378-401.	8.3	245
4	Analysis and architecture design of variable block-size motion estimation for H.264/AVC. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 578-593.	0.1	209
5	Flipping Structure: An Efficient VLSI Architecture for Lifting-Based Discrete Wavelet Transform. IEEE Transactions on Signal Processing, 2004, 52, 1080-1089.	5.3	182
6	Analysis and architecture design of block-coding engine for EBCOT in JPEG 2000. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 219-230.	8.3	178
7	Analysis and complexity reduction of multiple reference frames motion estimation in H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 507-522.	8.3	151
8	An efficient and simple VLSI tree architecture for motion estimation algorithms. IEEE Transactions on Signal Processing, 1993, 41, 889-900.	5.3	129
9	Survey on Block Matching Motion Estimation Algorithms and Architectures with New Results. Journal of Signal Processing Systems, 2006, 42, 297-320.	1.0	128
10	An efficient architecture for two-dimensional discrete wavelet transform. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 536-545.	8.3	126
11	Error concealment of lost motion vectors with overlapped motion compensation. IEEE Transactions on Circuits and Systems for Video Technology, 1997, 7, 560-563.	8.3	122
12	Fast Video Segmentation Algorithm With Shadow Cancellation, Global Motion Compensation, and Adaptive Threshold Techniques. IEEE Transactions on Multimedia, 2004, 6, 732-748.	7.2	107
13	Level C+ data reuse scheme for motion estimation with corresponding coding orders. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 553-558.	8.3	102
14	A 1.3TOPS H.264/AVC single-chip encoder for HDTV applications. , 0, , .		89
15	Fast Algorithm and Architecture Design of Low-Power Integer Motion Estimation for H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 568-577.	8.3	85
16	A novel 2Dd-to-3D conversion system using edge information. IEEE Transactions on Consumer Electronics, 2010, 56, 1739-1745.	3.6	84
17	Motion adaptive interpolation with horizontal motion detection for deinterlacing. IEEE Transactions on Consumer Electronics, 2003, 49, 1256-1265.	3.6	82
18	A cost-effective architecture for 8Ã—8 two-dimensional DCT/IDCT using direct method. IEEE Transactions on Circuits and Systems for Video Technology, 1997, 7, 459-467.	8.3	80

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19	A new block-matching criterion for motion estimation and its implementation. IEEE Transactions on Circuits and Systems for Video Technology, 1995, 5, 231-236.	8.3	78
20	Generic RAM-based architectures for two-dimensional discrete wavelet transform with line-based method. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 910-920.	8.3	76
21	An efficient parallel motion estimation algorithm for digital image processing. IEEE Transactions on Circuits and Systems for Video Technology, 1991, 1, 378-385.	8.3	73
22	Fully utilized and reusable architecture for fractional motion estimation of H.264/AVC. , 0, , .		70
23	Parallel 4Ã—4 2D transform and inverse transform architecture for MPEG-4 AVC/H.264. , 0, , .		66
24	Global Elimination Algorithm and Architecture Design for Fast Block Matching Motion Estimation. IEEE Transactions on Circuits and Systems for Video Technology, 2004, 14, 898-907.	8.3	65
25	Analysis and VLSI architecture for 1-D and 2-D discrete wavelet transform. IEEE Transactions on Signal Processing, 2005, 53, 1575-1586.	5.3	65
26	Architecture design for deblocking filter in H.264/JVT/AVC. , 2003, , .		64
27	Efficient Depth Image Based Rendering with Edge Dependent Depth Filter and Interpolation. , 0, , .		64
28	A data-interlacing architecture with two-dimensional data-reuse for full-search block-matching algorithm. IEEE Transactions on Circuits and Systems for Video Technology, 1998, 8, 124-127.	8.3	63
29	Predictive watershed: a fast watershed algorithm for video segmentation. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 453-461.	8.3	63
30	Accuracy improvement and cost reduction of 3-step search block matching algorithm for video coding. IEEE Transactions on Circuits and Systems for Video Technology, 1994, 4, 88-90.	8.3	61
31	A single-chip CMOS APS camera with direct frame difference output. IEEE Journal of Solid-State Circuits, 1999, 34, 1415-1418.	5.4	60
32	Lifting based discrete wavelet transform architecture for JPEG2000. , 0, , .		60
33	A 212 MPixels/s 4096 $imes$ 2160p Multiview Video Encoder Chip for 3D/Quad Full HDTV Applications. IEEE Journal of Solid-State Circuits, 2010, 45, 46-58.	5.4	60
34	Hardware-Efficient Belief Propagation. IEEE Transactions on Circuits and Systems for Video Technology, 2011, 21, 525-537.	8.3	60
35	Hardware architecture design for variable block size motion estimation in MPEG-4 AVC/JVT/ITU-T H.264. , 0, , .		58
36	System design consideration for digital wheelchair controller. IEEE Transactions on Industrial Electronics, 2000, 47, 898-907.	7.9	57

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37	Video de-interlacing by adaptive 4-field global/local motion compensated approach. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1569-1582.	8.3	55
38	Multimode Embedded Compression Codec Engine for Power-Aware Video Coding System. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 141-150.	8.3	54
39	Power-aware multimedia: concepts and design perspectives. IEEE Circuits and Systems Magazine, 2007, 7, 26-34.	2.3	50
40	Advances in Hardware Architectures for Image and Video Coding - A Survey. Proceedings of the IEEE, 2005, 93, 184-197.	21.3	48
41	Block-based Vanishing Line and Vanishing Point Detection for 3D Scene Reconstruction. , 2006, , .		48
42	Depth Map Generation for 2D-to-3D Conversion by Short-Term Motion Assisted Color Segmentation. , 2007, , .		47
43	A Localized Approach to Abandoned Luggage Detection with Foreground-Mask Sampling. , 2008, , .		46
44	A novel low-power full-search block-matching motion-estimation design for H.263+. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 890-897.	8.3	45
45	Analysis and reduction of reference frames for motion estimation in MPEG-4 AVC/JVT/H.264. , 0, , .		45
46	Content-Aware Prediction Algorithm With Inter-View Mode Decision for Multiview Video Coding. IEEE Transactions on Multimedia, 2008, 10, 1553-1564.	7.2	44
47	Analysis and design of macroblock pipelining for H.264/AVC VLSI architecture. , 0, , .		42
48	Seizure prediction based on classification of EEG synchronization patterns with on-line retraining and post-processing scheme. , 2011, 2011, 7564-9.		40
49	Architecture Design of H.264/AVC Decoder with Hybrid Task Pipelining for High Definition Videos. , 0, , .		38
50	Efficient VLSI architectures of lifting-based discrete wavelet transform by systematic design method. , 0, , .		37
51	Generic RAM-based architecture for two-dimensional discrete wavelet transform with line-based method. , 0, , .		37
52	iVisual: An Intelligent Visual Sensor SoC With 2790 fps CMOS Image Sensor and 205 GOPS/W Vision Processor. IEEE Journal of Solid-State Circuits, 2009, 44, 127-135.	5.4	37
53	An H.264/AVC scalable extension and high profile HDTV 1080p encoder chip. , 2008, , .		36
54	Bandwidth optimized motion compensation hardware design for H.264/AVC HDTV decoder. , 2005, , .		35

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55	A real-time 1080p 2D-to-3D video conversion system. IEEE Transactions on Consumer Electronics, 2011, 57, 915-922.	3.6	35
56	IC design of an adaptive Viterbi decoder. IEEE Transactions on Consumer Electronics, 1996, 42, 52-62.	3.6	34
57	Low-delay and error-robust wireless video transmission for video communications. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 1049-1058.	8.3	34
58	Parallel embedded block coding architecture for JPEG 2000. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1086-1097.	8.3	34
59	Algorithm and Architecture Design of Power-Oriented H.264/AVC Baseline Profile Encoder for Portable Devices. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1118-1128.	8.3	34
60	High speed memory efficient EBCOT architecture for JPEG2000. , 0, , .		33
61	Partial-result-reuse architecture and its design technique for morphological operations with flat structuring elements. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 1156-1169.	8.3	29
62	Analysis and architecture design of EBCOT for JPEG-2000. , 0, , .		28
63	2.8 to 67.2mW Low-Power and Power-Aware H.264 Encoder for Mobile Applications. , 2007, , .		28
64	A 52 mW Full HD 160-Degree Object Viewpoint Recognition SoC With Visual Vocabulary Processor for Wearable Vision Applications. IEEE Journal of Solid-State Circuits, 2012, 47, 797-809.	5.4	28
65	Dual-block-pipelined VLSI architecture of entropy coding for H.264/AVC baseline profile. , 0, , .		27
66	A 59.5mW scalable/multi-view video decoder chip for Quad/3D Full HDTV and video streaming applications. , 2010, , .		27
67	VLSI implementation of a selective median filter. IEEE Transactions on Consumer Electronics, 1996, 42, 33-42.	3.6	26
68	Joint Prediction Algorithm and Architecture for Stereo Video Hybrid Coding Systems. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 1324-1337.	8.3	26
69	An MPEG audio decoder chip. IEEE Transactions on Consumer Electronics, 1995, 41, 89-96.	3.6	25
70	VLSI Architecture for Forward Discrete Wavelet Transform Based on B-spline Factorization. Journal of Signal Processing Systems, 2005, 40, 343-353.	1.0	24
71	One-pass computation-aware motion estimation with adaptive search strategy. IEEE Transactions on Multimedia, 2006, 8, 698-706.	7.2	24
72	A 2D-to-3D conversion system using edge information. , 2010, , .		24

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73	A Low-power Low-voltage Direct Digital Frequency Synthesizer. , 0, , .		22
74	Hybrid motion/depth-oriented inpainting for virtual view synthesis in multiview applications. , 2010, , .		22
75	Performance analysis and architecture evaluation of MPEG-4 video codec system. , 0, , .		21
76	Single Reference Frame Multiple Current Macroblocks Scheme for Multiple Reference Frame Motion Estimation in H.264/AVC. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 242-247.	8.3	21
77	On-line empirical mode decomposition biomedical microprocessor for Hilbert Huang transform. , 2011, , .		21
78	Real-Time Depth Image based Rendering Hardware Accelerator for Advanced Three Dimensional Television System. , 2006, , .		20
79	On-Chip Memory Optimization Scheme for VLSI Implementation of Line-Based Two-Dimentional Discrete Wavelet Transform. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 814-822.	8.3	20
80	Fast motion estimation with inter-view motion vector prediction for stereo and multiview video coding. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	20
81	A block-based 2D-to-3D conversion system with bilateral filter. , 2009, , .		20
82	Visual Vocabulary Processor Based on Binary Tree Architecture for Real-Time Object Recognition in Full-HD Resolution. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2329-2332.	3.1	19
83	Computation reduction technique for lossy JPEG2000 encoding through EBCOT Tier-2 feedback processing. , 0, , .		18
84	Predictive line search: an efficient motion estimation algorithm for MPEG-4 encoding systems on multimedia processors. IEEE Transactions on Circuits and Systems for Video Technology, 2003, 13, 111-117.	8.3	18
85	Architecture design of full HD JPEG XR encoder for digital photography applications. IEEE Transactions on Consumer Electronics, 2008, 54, 963-971.	3.6	18
86	Single-iteration full-search fractional motion estimation for quad full HD H.264/AVC encoding. , 2009, , .		17
87	Localized Detection of Abandoned Luggage. Eurasip Journal on Advances in Signal Processing, 2010, 2010, .	1.7	17
88	Reconfigurable Morphological Image Processing Accelerator for Video Object Segmentation. Journal of Signal Processing Systems, 2011, 62, 77-96.	2.1	17
89	Low Power Cache Algorithm and Architecture Design for Fast Motion Estimation in H.264/AVC Encoder System. , 2007, , .		16
90	Architecture design of high performance embedded compression for high definition video coding. , 2008, , .		16

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91	128-channel spike sorting processor with a parallel-folding structure in 90nm process. , 2009, , .		16
92	A branch selection multi-symbol high throughput CABAC decoder architecture for H.264/AVC. , 2009, , .		16
93	Vector quantization using tree-structured self-organizing feature maps. IEEE Journal on Selected Areas in Communications, 1994, 12, 1594-1599.	14.0	15
94	A high quality MC-OBTC Codec for video signal processing. IEEE Transactions on Circuits and Systems for Video Technology, 1994, 4, 92-98.	8.3	15
95	Rate-optimal DSP synthesis by pipeline and minimum unfolding. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1994, 2, 81-88.	3.1	15
96	Performance analysis of hardware oriented algorithm modification in H.264. , 2003, , .		15
97	Memory analysis and architecture for two-dimensional discrete wavelet transform. , 0, , .		15
98	iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor. , 2008, , .		15
99	Cache-based integer motion/disparity estimation for quad-HD H.264/AVC and HD multiview video coding. , 2009, , .		15
100	Video stabilization for vehicular applications using SURF-like descriptor and KD-tree. , 2010, , .		15
101	Channel selection for epilepsy seizure prediction method based on machine learning. , 2012, 2012, 5162-5.		15
102	Analysis of EBCOT decoding algorithm and its VLSI implementation for JPEG 2000. , 0, , .		14
103	An efficient and low power architecture design for motion estimation using global elimination algorithm. , 2002, , .		14
104	Hardware architecture design for H.264/AVC intra frame coder. , 0, , .		14
105	Reconfigurable Discrete Wavelet Transform Processor for Heterogeneous Reconfigurable Multimedia Systems. Journal of Signal Processing Systems, 2005, 41, 35-47.	1.0	14
106	Relative Depth Layer Extraction for Monoscopic Video by Use of Multidimensional Filter. , 2006, , .		14
107	Hardware-efficient belief propagation. , 2009, , .		14
108	A multimedia semantic analysis SoC (SASoC) with machine-learning engine. , 2010, , .		14

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109	A flexible fully hardwired CABAC encoder for UHDTV H.264/AVC high profile video. IEEE Transactions on Consumer Electronics, 2012, 58, 1329-1337.	3.6	14
110	ASG: Automatic schematic generator. The Integration VLSI Journal, 1991, 11, 11-27.	2.1	13
111	A digital signal processor with programmable correlator array architecture for third generation wireless communication system. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2001, 48, 1110-1120.	2.2	13
112	Error concealment algorithm using interested direction for JPEG 2000 image transmission. IEEE Transactions on Consumer Electronics, 2003, 49, 1395-1401.	3.6	13
113	High performance two-symbol arithmetic encoder in JPEG 2000. , 0, , .		13
114	Multi-mode embedded compression codec engine for power-aware video coding system. , 0, , .		13
115	Low Power Entropy Coding Hardware Design for H.264/AVC Baseline Profile Encoder. , 2006, , .		13
116	Extended intelligent edge-based line average with its implementation and test method. , 0, , .		12
117	A multimedia video conference system: using region base hybrid coding. IEEE Transactions on Consumer Electronics, 1996, 42, 781-786.	3.6	12
118	A VLSI architecture design of VLC encoder for high data rate video/image coding. , 0, , .		12
119	Efficient video segmentation algorithm for real-time MPEG-4 camera system. , 2000, , .		12
120	Analysis and architecture design of lifting based DWT and EBCOT for JPEG 2000. , 0, , .		12
121	A Programmable Parallel VLSI Architecture for 2-D Discrete Wavelet Transform. Journal of Signal Processing Systems, 2001, 28, 151-163.	1.0	12
122	A novel hybrid motion estimator supporting diamond search and fast full search. , 0, , .		12
123	Low-power parallel tree architecture for full search block-matching motion estimation. , 0, , .		12
124	Bandwidth-efficient cache-based motion compensation architecture with DRAM-friendly data access control. , 2009, , .		12
125	Low power full-search block-matching motion estimation chip for H.263+. , 0, , .		11
126	A Low Power 8 x 8 Direct 2-D DCT Chip Design. Journal of Signal Processing Systems, 2000, 26, 319-332.	1.0	11

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127	Four field local motion compensated de-interlacing. , 0, , .		11
128	Novel precompression rate-distortion optimization algorithm for JPEG 2000. , 2004, , .		11
129	Stereo Video Coding System with Hybrid Coding Based on Joint Prediction Scheme. , 0, , .		11
130	Precompression Quality-Control Algorithm for JPEG 2000. IEEE Transactions on Image Processing, 2006, 15, 3279-3293.	9.8	11
131	System Analysis of VLSI Architecture for 5/3 and 1/3 Motion-Compensated Temporal Filtering. IEEE Transactions on Signal Processing, 2006, 54, 4004-4014.	5.3	11
132	Algorithm analysis and architecture design for HDTV applications. IEEE Circuits and Devices: the Magazine of Electronic and Photonic Systems, 2006, 22, 22-31.	0.4	11
133	Low power and power aware fractional motion estimation of H.264/AVC for mobile applications. , 0, , .		11
134	VLSI Architecture Design of Fractional Motion Estimation for H.264/AVC. Journal of Signal Processing Systems, 2008, 53, 335-347.	2.1	11
135	Priority depth fusion for the 2D to 3D conversion system. Proceedings of SPIE, 2008, , .	0.8	11
136	Pyramid Architecture for 3840 X 2160 Quad Full High Definition 30 Frames/s Video Acquisition. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1499-1508.	8.3	11
137	Accurate and Bandwidth Efficient Architecture for CNN-based Full-HD Super-Resolution. , 2018, , .		11
138	A real-time video signal processing chip. IEEE Transactions on Consumer Electronics, 1993, 39, 82-92.	3.6	10
139	A programmable VLSI architecture for 2-D discrete wavelet transform. , 0, , .		10
140	Bit-plane error recovery via cross subband for image transmission in JPEG2000. , 0, , .		10
141	Multi-Mode Content-Aware Motion Estimation Algorithm for Power-Aware Video Coding Systems. , 0, , .		10
142	Single Reference Frame Multiple Current Macroblocks Scheme for Multi-Frame Motion Estimation in H.264/AVC. , 0, , .		10
143	Hardware architecture design of an H.264/AVC video codec. , 0, , .		10
144	Architecture Design of Area-Efficient SRAM-Based Multi-Symbol Arithmetic Encoder in H.264/AVC. , 0, , .		10

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145	Single iteration view interpolation for multiview video applications. , 2009, , .		10
146	Architecture design of stereo matching using belief propagation. , 2010, , .		10
147	A 69mW 140-meter/60fps and 60-meter/300fps intelligent vision SoC for versatile automotive applications. , 2012, , .		10
148	An intelligent depth-based obstacle detection system for visually-impaired aid applications. , 2012, , .		10
149	23.2 A 1920×1080 30fps 611 mW five-view depth-estimation processor for light-field applications. , 2015, , .		10
150	Concurrent error-detectable butterfly chip for real-time FFT processing through time redundancy. IEEE Journal of Solid-State Circuits, 1993, 28, 537-547.	5.4	9
151	A 32-bit logarithmic number system processor. Journal of Signal Processing Systems, 1996, 14, 311-319.	1.0	9
152	A novel MPEG-2 audio decoder with efficient data arrangement and memory configuration. IEEE Transactions on Consumer Electronics, 1997, 43, 598-604.	3.6	9
153	Scalable module-based architecture for MPEG-4 BMA motion estimation. , 0, , .		9
154	Design and implementation of a bitstream parsing coprocessor for MPEG-4 video system-on-chip solution. , 0, , .		9
155	VLSI implementation of shape-adaptive discrete wavelet transform. , 2002, , .		9
156	VLSI architecture design of MPEG-4 shape coding. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 741-751.	8.3	9
157	iVisual. , 2008, , .		9
158	51.3: An Ultra-Low-Cost 2-D/3-D Video-Conversion System. Digest of Technical Papers SID International Symposium, 2010, 41, 766.	0.3	9
159	Feature-based video stabilization for vehicular applications. , 2010, , .		9
160	An intelligent vision-based vehicle detection and tracking system for automotive applications. , 2011, , .		9
161	Efficient Hardware Architecture for Large Disparity Range Stereo Matching Based on Belief Propagation. , 2016, , .		9
162	A low power 2D DCT chip design using direct 2D algorithm. , 0, , .		8

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163	Flipping structure: an efficient VLSI architecture for lifting-based discrete wavelet transform. , 0, , .		8
164	Motion adaptive de-interlacing by horizontal motion detection and enhanced ELA processing. , 0, , .		8
165	An Efficient Embedded Bitstream Parsing Processor for MPEG-4 Video Decoding System. Journal of Signal Processing Systems, 2005, 41, 183-191.	1.0	8
166	Memory Analysis of VLSI Architecture for 5/3 and 1/3 Motion-Compensated Temporal Filtering. , 0, , .		8
167	Power-Scalable Algorithm and Reconfigurable Macro-Block Pipelining Architecture of H.264 Encoder for Mobile Application. , 2006, , .		8
168	High-performance JPEG 2000 encoder with rate-distortion optimization. IEEE Transactions on Multimedia, 2006, 8, 645-653.	7.2	8
169	System Bandwidth Analysis of Multiview Video Coding with Precedence Constraint. , 2007, , .		8
170	Computation-Free Motion Estimation with Inter-View Mode Decision for Multiview Video Coding. , 2007, , .		8
171	Data Reuse Exploration for Low Power Motion Estimation Architecture Design in H.264 Encoder. Journal of Signal Processing Systems, 2008, 50, 1-17.	2.1	8
172	Efficient Architecture Design of Motion-Compensated Temporal Filtering/Motion Compensated Prediction Engine. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 98-109.	8.3	8
173	Analysis of belief propagation for hardware realization. , 2008, , .		8
174	Fast belief propagation process element for high-quality stereo estimation. , 2009, , .		8
175	Hybrid depth cueing for 2D-to-3D conversion system. Proceedings of SPIE, 2009, , .	0.8	8
176	Multichannel evoked neural signal compression using advanced video compression algorithm. , 2009, , .		8
177	Accuracy and power tradeoff in spike sorting microsystems with cubic spline interpolation. , 2010, , .		8
178	Robust heart rate measurement with phonocardiogram by on-line template extraction and matching. , 2011, 2011, 1957-60.		8
179	A real-time system for object detection and location reminding with RGB-D camera. , 2014, , .		8
180	Fast realistic refocusing for sparse light fields. , 2015, , .		8

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181	A self-adjusting weighted median filter for removing impulse noise in images. , 0, , .		7
182	A novel image compression algorithm by using Log-Exp transform. , 0, , .		7
183	Design of a low power psycho-acoustic model co-processor for MPEG-2/4 AAC LC stereo encoder. , 0, , .		7
184	Power-efficient FIR filter architecture design for wireless embedded system. IEEE Transactions on Circuits and Systems II: Express Briefs, 2004, 51, 21-25.	3.0	7
185	A low complexity design of psycho-acoustic model for MPEG-2/4 advanced audio coding. IEEE Transactions on Consumer Electronics, 2004, 50, 1209-1217.	3.6	7
186	JPEG, MPEG-4, and H.264 Codec IP Development. , 0, , .		7
187	Memory Efficient JPEG 2000 Architecture with Stripe Pipeline Scheme. , 0, , .		7
188	Fast decomposition of filterbanks for the state-of-the-art audio coding. IEEE Signal Processing Letters, 2005, 12, 693-696.	3.6	7
189	Hardware oriented content-adaptive fast algorithm for variable block-size integer motion estimation in H.264. , 2005, , .		7
190	Novel Configurable Architecture of ML-Decomposed Binary Arithmetic Encoder for Multimedia Applications. , 2007, , .		7
191	A Quality-of-Experience Video Adaptor for Serving Scalable Video Applications. IEEE Transactions on Consumer Electronics, 2007, 53, 1130-1137.	3.6	7
192	Architecture Design of Fine Grain Quality Scalable Encoder with CABAC for H.264/AVC Scalable Extension. Journal of Signal Processing Systems, 2010, 60, 363-375.	2.1	7
193	Analysis and design of on-sensor ECG processors for realtime detection of VF, VT, and PVC. , 2010, , .		7
194	1.4µW/channel 16-channel EEG/ECoG processor for smart brain sensor SoC. , 2010, , .		7
195	Design and implementation of cubic spline interpolation for spike sorting microsystems. , 2011, , .		7
196	Brain-Inspired Framework for Fusion of Multiple Depth Cues. IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23, 1137-1149.	8.3	7
197	Object-oriented video coding algorithm for very low bit-rate system. , 0, , .		6
198	VLSI implementation of the motion estimator with two-dimensional data-reuse. IEEE Transactions on Consumer Electronics, 1998, 44, 623-629.	3.6	6

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199	Reconfigurable discrete wavelet transform architecture for advanced multimedia systems. , 0, , .		6
200	Motion compensated de-interlacing with adaptive global motion estimation and compensation. , 0, , .		6
201	Platform-based MPEG-4 video encoder SoC design. , 0, , .		6
202	Multiple-lifting Scheme: Memory-efficient VLSI Implementation for Line-based 2-D DWT. , 0, , .		6
203	Memory Efficient JPEG 2000 Architecture With Stripe Pipeline Scheduling. IEEE Transactions on Signal Processing, 2006, 54, 4807-4816.	5.3	6
204	Hybrid Morphology Processing Unit Architecture for Moving Object Segmentation Systems. Journal of Signal Processing Systems, 2006, 42, 241-255.	1.0	6
205	Bandwidth-Efficient Encoder Framework for H.264/AVC Scalable Extension. , 2007, , .		6
206	An 8.6mW 12.5Mvertices/s 800MOPS 8.91mm² Stream Processor Core for Mobile Graphics and Video Applications. , 2007, , .		6
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208	Pipelined arithmetic encoder design for lossless JPEG XR encoder. , 2009, , .		6
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211	Cubic spline interpolation with overlapped window and data reuse for on-line Hilbert Huang transform biomedical microprocessor. , 2011, 2011, 7091-4.		6
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214	A novel video signal processor with programmable data arrangement and efficient memory configuration. IEEE Transactions on Consumer Electronics, 1996, 42, 526-534.	3.6	5
215	Robust error concealment algorithm for MPEG-4 with the aid of fuzzy theory. , 0, , .		5
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