Ajith Pasqual

List of Publications by Year
in descending order

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24	136	2258059	2272923
papers	citations	3	4
		h-index	g-index

24	24	24	149
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Four-Step Method to Synthesize a DCâ€“DC Converter for Multi-Inductor Realizable Arbitrary Voltage Conversion Ratio. IEEE Transactions on Industrial Electronics, 2022, 69, 5594-5603.	7.9	6
2	Nonisolated DCâ€“DC Power Converter Synthesis Using Low-Entropy Equations. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022, 10, 6457-6469.	5.4	5
3	A Design Methodology to Synthesize First Degree Single-Path Hybrid DCâ€“DC Converters. IEEE Transactions on Power Electronics, 2022, 37, 12336-12345.	7.9	1
4	SMPTE ST 2110 Compliant Scalable Architecture on FPGA for end to end Uncompressed Professional Video Transport Over IP Networks. , 2019, , .		2
5	VLIW Based Runtime Reconfigurable Machine Vision Coprocessor Architecture for Edge Computing. , 2019, , .		0
6	EdgeNet: SqueezeNet like Convolution Neural Network on Embedded FPGA. , 2018, , .		10
7	An Analytical Method to Derive a DC-DC Converter for an Arbitrary Voltage Conversion Ratio. , 2018, , .		3
8	A Novel Low-Complexity VLSI Architecture for an EEG Feature Extraction Platform. , 2018, , .		4
9	Reconfigurable co-processor architecture with limited numerical precision to accelerate deep convolutional neural networks. , 2018, , .		5
10	Runtime rule-reconfigurable high throughput NIPS on FPGA. , 2017, , .		5
11	FPAA and FPGA based universal sensor node design. , 2017, , .		1
12	Micro Actions and Deep Static Features for Activity Recognition. , 2017, , .		0
13	Real time all intra HEVC HD encoder on FPGA. , 2016, , .		13
14	High performance flow matching architecture for OpenFlow data plane. , 2016, , .		3
15	4K Real-Time HEVC Decoder on an FPGA. IEEE Transactions on Circuits and Systems for Video Technology, 2016, 26, 236-249.	8.3	40
16	HEVC inverse transform architecture utilizing coefficient sparsity. , 2015, , .		0
17	FPGA based custom accelerator architecture framework for complex event processing. , 2014, , .		1
18	Online classification of imagined hand movement using a consumer grade EEG device. , 2013, , .		10

#	Article	IF	Citations
19	Line rate parallel packet classification module for NetFPGA platform. , 2013, , .		1
20	High performance parallel packet Classification architecture with Popular Rule Caching. , 2012, , .		7
21	HLS approach in designing FPGA-based custom coprocessor for image preprocessing. , 2010, , .		5
22	Scalable FPGA-based multiprocessor architecture for real-time embedded vision. , 2010, , .		1
23	FPGA-based compact and flexible architecture for real-time embedded vision systems. , 2009, , .		9
24	Impact of ICT on learning and teaching. , 2008, , .		4