Mohammad Hossein Moaiyeri

List of Publications by Year
in descending order

143 papers	3,234 citations	147726 31 h-index	206029 48 g-index
144 all docs	144 docs citations	144 times ranked	955 citing authors

#	Article	IF	Citations
1	Design of energy-efficient and robust ternary circuits for nanotechnology. IET Circuits, Devices and Systems, 2011, 5, 285.	0.9	200
2	Designing efficient QCA logical circuits with power dissipation analysis. Microelectronics Journal, 2015, 46, 462-471.	1.1	142
3	A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4200-4208.	3.5	118
4	Two new low-power Full Adders based on majority-not gates. Microelectronics Journal, 2009, 40, 126-130.	1.1	107
5	A universal method for designing lowâ€power carbon nanotube FETâ€based multipleâ€valued logic circuits. IET Computers and Digital Techniques, 2013, 7, 167-181.	0.9	90
6	Energy and area efficient imprecise compressors for approximate multiplication at nanoscale. AEU - International Journal of Electronics and Communications, 2019, 110, 152859.	1.7	75
7	Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics. Nano-Micro Letters, 2011, 3, 43-50.	14.4	68
8	Designing quantum-dot cellular automata counters with energy consumption analysis. Microprocessors and Microsystems, 2015, 39, 512-520.	1.8	65
9	Design and Evaluation of CNFET-Based Quaternary Circuits. Circuits, Systems, and Signal Processing, 2012, 31, 1631-1652.	1.2	62
10	Design and Evaluation of an Efficient Schmitt Trigger-Based Hardened Latch in CNTFET Technology. IEEE Transactions on Device and Materials Reliability, 2017, 17, 267-277.	1.5	61
11	A low-power single-ended SRAM in FinFET technology. AEU - International Journal of Electronics and Communications, 2019, 99, 361-368.	1.7	54
12	Performance analysis and enhancement of 10-nm GAA CNTFET-based circuits in the presence of CNT-metal contact resistance. Journal of Computational Electronics, 2017, 16, 240-252.	1.3	53
13	An energy and cost efficient majority-based RAM cell in quantum-dot cellular automata. Results in Physics, 2017, 7, 3543-3551.	2.0	49
14	Design and analysis of a high-performance CNFET-based Full Adder. International Journal of Electronics, 2012, 99, 113-130.	0.9	48
15	Novel Efficient Adder Circuits for Quantum-Dot Cellular Automata. Journal of Computational and Theoretical Nanoscience, 2011, 8, 1769-1775.	0.4	47
16	An efficient majority-based compressor for approximate computing in the nano era. Microsystem Technologies, 2018, 24, 1589-1601.	1.2	47
17	A Variation-Aware Ternary Spin-Hall Assisted STT-RAM Based on Hybrid MTJ/GAA-CNTFET Logic. IEEE Nanotechnology Magazine, 2019, 18, 598-605.	1.1	47
18	Design and implementation of Multistage Interconnection Networks using Quantum-dot Cellular Automata. Microelectronics Journal, 2011, 42, 913-922.	1.1	46

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19	Active Shielding of MWCNT Bundle Interconnects: An Efficient Approach to Cancellation of Crosstalk-Induced Functional Failures in Ternary Logic. IEEE Transactions on Electromagnetic Compatibility, 2019, 61, 100-110.	1.4	46
20	Quantum-dot cellular automata circuits with reduced external fixed inputs. Microprocessors and Microsystems, 2017, 50, 154-163.	1.8	44
21	Design of an ultra-efficient reversible full adder-subtractor in quantum-dot cellular automata. Optik, 2017, 142, 557-563.	1.4	43
22	Novel direct designs for 3-input XOR function for low-power and high-speed applications. International Journal of Electronics, 2010, 97, 647-662.	0.9	42
23	An energy and area efficient 4:2 compressor based on FinFETs. The Integration VLSI Journal, 2018, 60, 224-231.	1.3	42
24	Efficient Passive Shielding of MWCNT Interconnects to Reduce Crosstalk Effects in Multiple-Valued Logic Circuits. IEEE Transactions on Electromagnetic Compatibility, 2019, 61, 1593-1601.	1.4	42
25	Robust and energy-efficient carbon nanotube FET-based MVL gates: A novel design approach. Microelectronics Journal, 2015, 46, 1333-1342.	1.1	40
26	An Ultra-Low-Power 9T SRAM Cell Based on Threshold Voltage Techniques. Circuits, Systems, and Signal Processing, 2016, 35, 1437-1455.	1.2	40
27	Comparative Analysis of Simultaneous Switching Noise Effects in MWCNT Bundle and Cu Power Interconnects in CNTFET-Based Ternary Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 37-46.	2.1	39
28	An efficient ternary serial adder based on carbon nanotube FETs. Engineering Science and Technology, an International Journal, 2016, 19, 271-278.	2.0	38
29	Comparative Analysis of the Crosstalk Effects in Multilayer Graphene Nanoribbon and MWCNT Interconnects in Sub-10 nm Technologies. IEEE Transactions on Electromagnetic Compatibility, 2020, 62, 561-570.	1.4	35
30	Ultra-Compact Ternary Logic Gates Based on Negative Capacitance Carbon Nanotube FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2162-2166.	2.2	35
31	A robust and low-power near-threshold SRAM in 10-nm FinFET technology. Analog Integrated Circuits and Signal Processing, 2018, 94, 497-506.	0.9	33
32	Process-in-Memory Using a Magnetic-Tunnel-Junction Synapse and a Neuron Based on a Carbon Nanotube Field-Effect Transistor. IEEE Magnetics Letters, 2019, 10, 1-5.	0.6	33
33	Analysis of Crosstalk Effects for Multiwalled Carbon Nanotube Bundle Interconnects in Ternary Logic and Comparison with Cu interconnects. IEEE Nanotechnology Magazine, 2016, , 1-1.	1.1	31
34	Nonvolatile Associative Memory Design Based on Spintronic Synapses and CNTFET Neurons. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 428-437.	3.2	31
35	A low-voltage and energy-efficient full adder cell based on carbon nanotube technology. Nano-Micro Letters, 2010, 2, 114-120.	14.4	30
36	Quaternary full adder cells based on carbon nanotube FETs. Journal of Computational Electronics, 2015, 14, 762-772.	1.3	29

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37	An Energy-Efficient Full Adder Cell Using CNFET Technology. IEICE Transactions on Electronics, 2012, E95.C, 744-751.	0.3	28
38	Efficient and Robust SRAM Cell Design Based on Quantum-Dot Cellular Automata. ECS Journal of Solid State Science and Technology, 2018, 7, Q38-Q45.	0.9	28
39	A NEW ROBUST AND HIGH-PERFORMANCE HYBRID FULL ADDER CELL. Journal of Circuits, Systems and Computers, 2011, 20, 641-655.	1.0	27
40	Design and evaluation of energy-efficient carbon nanotube FET-based quaternary minimum and maximum circuits. Journal of Applied Research and Technology, 2017, 15, 233-241.	0.6	27
41	Ultra-Efficient Fuzzy Min/Max Circuits Based on Carbon Nanotube FETs. IEEE Transactions on Fuzzy Systems, 2018, 26, 1073-1078.	6.5	27
42	Computational Investigation of Negative Capacitance Coaxially Gated Carbon Nanotube Field-Effect Transistors. IEEE Transactions on Electron Devices, 2021, 68, 376-384.	1.6	27
43	High-speed full adder based on minority function and bridge style for nanoscale. The Integration VLSI Journal, 2011, 44, 155-162.	1.3	26
44	Impacts of Process and Temperature Variations on the Crosstalk Effects in Sub-10 nm Multilayer Graphene Nanoribbon Interconnects. IEEE Transactions on Device and Materials Reliability, 2019, 19, 630-641.	1.5	26
45	True Random Number Generator for Reliable Hardware Security Modules Based on a Neuromorphic Variation-Tolerant Spintronic Structure. IEEE Nanotechnology Magazine, 2020, 19, 784-791.	1.1	26
46	High-Performance Spintronic Nonvolatile Ternary Flip-Flop and Universal Shift Register. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 916-924.	2.1	26
47	High-Performance Mixed-Mode Universal Min-Max Circuits for Nanotechnology. Circuits, Systems, and Signal Processing, 2012, 31, 465-488.	1.2	25
48	High Performance CNFET-based Ternary Full Adders. IETE Journal of Research, 2018, 64, 108-115.	1.8	25
49	Leveraging Negative Capacitance CNTFETs for Image Processing: An Ultra-Efficient Ternary Image Edge Detection Hardware. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 5108-5119.	3.5	25
50	Two New Low-Power and High-Performance Full Adders. Journal of Computers, 2009, 4, .	0.4	24
51	Dramatically Low-Transistor-Count High-Speed Ternary Adders. , 2013, , .		23
52	A hardware-friendly arithmetic method and efficient implementations for designing digital fuzzy adders. Fuzzy Sets and Systems, 2011, 185, 111-124.	1.6	20
53	High-Performance Radiation-Hardened Spintronic Retention Latch and Flip-Flop for Highly Reliable Processors. IEEE Transactions on Device and Materials Reliability, 2021, 21, 215-223.	1.5	20
54	CNFET-based approximate ternary adders for energy-efficient image processing applications. Microprocessors and Microsystems, 2016, 47, 454-465.	1.8	19

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55	Effective Reduction in Crosstalk Effects in Quaternary Integrated Circuits Using Mixed Carbon Nanotube Bundle Interconnects. ECS Journal of Solid State Science and Technology, 2018, 7, M69-M76.	0.9	19
56	Carbon Nanotube Field Effect Transistor Switching Logic for Designing Efficient Ternary Arithmetic Circuits. Journal of Nanoelectronics and Optoelectronics, 2017, 12, 118-129.	0.1	19
57	Energy- and Quality-Efficient Approximate Multipliers for Neural Network and Image Processing Applications. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	18
58	An efficient approach to enhance bulk-driven amplifiers. Analog Integrated Circuits and Signal Processing, 2017, 92, 489-499.	0.9	17
59	A low-power dynamic ternary full adder using carbon nanotube field-effect transistors. AEU - International Journal of Electronics and Communications, 2021, 131, 153600.	1.7	17
60	Analog/RF performance assessment of ferroelectric junctionless carbon nanotube FETs: A quantum simulation study. Physica E: Low-Dimensional Systems and Nanostructures, 2021, 134, 114915.	1.3	17
61	An Ultra-Low-Power and Robust Ternary Static Random Access Memory Cell Based on Carbon Nanotube FETs. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 617-627.	0.1	17
62	Ultra high speed Full Adders. IEICE Electronics Express, 2008, 5, 744-749.	0.3	16
63	Comparative Performance Evaluation of Large FPGAs with CNFET- and CMOS-based Switches in Nanoscale. Nano-Micro Letters, 2011, 3, 178-188.	14.4	16
64	Design of Efficient and Testable <I>n</I>-Input Logic Gates in Quantum-Dot Cellular Automata. Journal of Computational and Theoretical Nanoscience, 2013, 10, 2347-2353.	0.4	16
65	Design and analysis of carbon nanotube FET based quaternary full adders. Frontiers of Information Technology and Electronic Engineering, 2016, 17, 1056-1066.	1.5	16
66	On the Impacts of Process and Temperature Variations on the Crosstalk Effects in MWCNT Bundle Nanointerconnects in Ternary Logic. IEEE Nanotechnology Magazine, 2018, 17, 238-249.	1.1	16
67	BVA-NQSL: A Bio-Inspired Variation-Aware Nonvolatile Quaternary Spintronic Latch. IEEE Magnetics Letters, 2020, 11, 1-5.	0.6	16
68	Bio-Inspired Nonvolatile and Low-Cost Spin-Based 2-Bit Per Cell Memory. , 2020, , .		16
69	Ultra-Efficient Nonvolatile Approximate Full-Adder With Spin-Hall-Assisted MTJ Cells for In-Memory Computing Applications. IEEE Transactions on Magnetics, 2021, 57, 1-11.	1.2	16
70	Low-Cost Implementation of Bilinear and Bicubic Image Interpolation for Real-Time Image Super-Resolution. , 2020, , .		16
71	On the design of new low-power CMOS standard ternary logic gates. , 2010, , .		15
72	A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology. Journal of Computational Electronics, 2019, 18, 519-526.	1.3	15

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73	Energy-efficient magnetic approximate full adder with spin-Hall assistance for signal processing applications. Analog Integrated Circuits and Signal Processing, 2020, 102, 645-657.	0.9	15
74	Efficient and Highly Reliable Spintronic Non-volatile Quaternary Memory Based on Carbon Nanotube FETs and Multi-TMR MTJs. ECS Journal of Solid State Science and Technology, 2022, 11, 061007.	0.9	15
75	Efficient Single-Electron Transistor Inverter-Based Logic Circuits and Memory Elements. Journal of Computational and Theoretical Nanoscience, 2013, 10, 1171-1178.	0.4	14
76	An Energy- and Area-Efficient Approximate Ternary Adder Based on CNTFET Switching Logic. Circuits, Systems, and Signal Processing, 2018, 37, 1863-1883.	1.2	14
77	Ultra-Compact Imprecise 4:2 Compressor and Multiplier Circuits for Approximate Computing in Deep Nanoscale. Circuits, Systems, and Signal Processing, 2021, 40, 4633-4650.	1.2	14
78	CNFET-based design of efficient ternary half adder and 1-trit multiplier circuits using dynamic logic. Microelectronics Journal, 2021, 113, 105105.	1.1	14
79	Design and evaluation of a 5-input majority gate-based content-addressable memory cell in quantum-dot cellular automata. , 2017, , .		13
80	A novel digital fuzzy system for image edge detection based on wrap-gate carbon nanotube transistors. Computers and Electrical Engineering, 2020, 87, 106811.	3.0	12
81	Ultraefficient imprecise multipliers based on innovative 4:2 approximate compressors. International Journal of Circuit Theory and Applications, 2021, 49, 169-184.	1.3	12
82	CNFET-Based Design of Energy-Efficient Symmetric Three-Input XOR and Full Adder Circuits. Arabian Journal for Science and Engineering, 2013, 38, 3367-3382.	1.1	11
83	An Energy-Efficient and Robust Voltage Level Converter for Nanoelectronics. International Journal of Modern Education and Computer Science, 2015, 7, 1-7.	2.4	11
84	A high-performance fully programmable membership function generator based on 10Ânm gate-all-around CNTFETs. AEU - International Journal of Electronics and Communications, 2020, 123, 153293.	1.7	11
85	Design of an Energy-Efficient Radiation-Hardened Non-Volatile Magnetic Latch. IEEE Transactions on Magnetics, 2021, 57, 1-10.	1.2	11
86	An Ultra High-Speed (4; 2) Compressor with a New Design Approach for Nanotechnology Based on the Multi-Input Majority Function. Journal of Computational and Theoretical Nanoscience, 2014, 11, 1691-1696.	0.4	10
87	Comparative analysis of adiabatic full adder cells in CNFET technology. Engineering Science and Technology, an International Journal, 2016, 19, 2119-2128.	2.0	10
88	MTMR-SNQM: Multi-Tunnel Magnetoresistance Spintronic Non-volatile Quaternary Memory. , 2021, , .		10
89	DDR-MRAM: Double Data Rate Magnetic RAM for Efficient Artificial Intelligence and Cache Applications. IEEE Transactions on Magnetics, 2022, 58, 1-9.	1.2	10
90	Five New MVL Current Mode Differential Absolute Value Circuits Based on Carbon Nano-tube Field Effect Transistors (CNTFETs). Nano-Micro Letters, 2010, 2, 227-234.	14.4	9

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91	A new SPICE model for organic molecular transistors and a novel hybrid architecture. IEICE Electronics Express, 2012, 9, 926-931.	0.3	8
92	A Low-Power Multiplier Using an Efficient Single-Supply Voltage Level Converter. Journal of Circuits, Systems and Computers, 2015, 24, 1550124.	1.0	8
93	Ultra-low-power carbon nanotube FET-based quaternary logic gates. International Journal of Electronics, 0, , 1-14.	0.9	8
94	A low-power and area-efficient quaternary adder based on CNTFET switching logic. Analog Integrated Circuits and Signal Processing, 2019, 98, 221-232.	0.9	8
95	Design of an efficient fully nonvolatile and radiation-hardened majority-based magnetic full adder using FinFET/MTJ. Microelectronics Journal, 2020, 103, 104864.	1.1	8
96	A high-performance low-voltage current-mode min/max circuit. COMPEL - the International Journal for Computation and Mathematics in Electrical and Electronic Engineering, 2015, 34, 1172-1183.	0.5	7
97	On the design of quaternary arithmetic logic unit based on CNTFETs. International Journal of Electronics Letters, 2019, 7, 1-13.	0.7	7
98	NVLCFF: An Energy-Efficient Magnetic Nonvolatile Level Converter Flip-Flop for Ultra-Low-Power Design. Circuits, Systems, and Signal Processing, 2020, 39, 2841-2859.	1.2	7
99	A Task-Schedulable Nonvolatile Spintronic Field-Programmable Gate Array. IEEE Magnetics Letters, 2021, 12, 1-4.	0.6	7
100	Breaking the Limits in Ternary Logic: An Ultra-Efficient Auto-Backup/Restore Nonvolatile Ternary Flip-Flop Using Negative Capacitance CNTFET Technology. IEEE Access, 2021, 9, 132641-132651.	2.6	7
101	A high-performance 5-to-2 compressor cell based on carbon nanotube FETs. International Journal of Electronics, 2019, 106, 912-927.	0.9	7
102	Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics. Nano-Micro Letters, 2011, 3, 43.	14.4	7
103	High-Performance and Soft Error Immune Spintronic Retention Latch for Highly Reliable Processors. , 2020, , .		7
104	An Efficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotube FETs. ETRI Journal, 2014, 36, 89-98.	1.2	6
105	High-performance ternary logic gates for nanoelectronics. International Journal of High Performance Systems Architecture, 2015, 5, 209.	0.2	6
106	Energy-efficient magnetic 5:2 compressors based on SHE-assisted hybrid MTJ/FinFET logic. Journal of Computational Electronics, 2020, 19, 206-221.	1.3	6
107	Magnetic nonvolatile flip-flops with spin-Hall assistance for power gating in ternary systems. Journal of Computational Electronics, 2020, 19, 1175-1186.	1.3	6
108	Stochastic Spintronic Neuron with Application to Image Binarization. , 2021, , .		6

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109	An Efficient Analog-to-Digital Converter Based on Carbon Nanotube FETs. Journal of Low Power Electronics, 2016, 12, 150-157.	0.6	6
110	Ultra low-power 7T SRAM cell design based on CMOS. , 2015, , .		5
111	Ultra-High-Performance Magnetic Nonvolatile Level Converter Flip-Flop with Spin-Hall Assistance for Dual-Supply Systems with Power Gating Architecture. Circuits, Systems, and Signal Processing, 2021, 40, 1383-1396.	1.2	5
112	Vertical Noise Reduction in 3-D Mixed-Signal Integrated Circuits With Graphene Nanoribbon and Carbon Nanotube Interconnects. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 302-311.	1.4	5
113	A Low-Voltage and Energy-Efficient Full Adder Cell Based on Carbon Nanotube Technology. Nano-Micro Letters, 2010, 2, 114.	14.4	5
114	Toward Efficient Logic-in-Memory Computing With Magnetic Reconfigurable Logic Circuits. IEEE Magnetics Letters, 2022, 13, 1-5.	0.6	5
115	Analytical performance evaluation of molecular logic circuits. , 2012, , .		4
116	An applicable high-efficient CNTFET-based full adder cell for practical environments. , 2012, , .		4
117	A low-voltage level shifter based on double-gate MOSFET. , 2015, , .		4
118	Design of CNTFET-based Current-mode Multi-input m:3 (4â€‰â‰€â€‰mâ€‰â‰€â€‰7) Counters. IETE Journal of Research, 2021, 67, 322-332.	1.8	4
119	New high-performance majority function based full adders. , 2009, , .		3
120	A New Full Adder Cell for Molecular Electronics. International Journal of VLSI Design & Communication Systems, 2011, 2, 1-13.	0.2	3
121	Efficient radix-radders for nanoelectronics. International Journal of Electronics, 2016, 103, 281-296.	0.9	3
122	Digital counter cell design using carbon nanotube FETs. Journal of Applied Research and Technology, 2017, 15, 211-222.	0.6	3
123	Comparative analysis of the impacts of CNTFET and GNRFET drivers on the crosstalk effects in MLGNR interconnects at 7nm technology node. , 2020, , .		3
124	Ultra-Efficient and Robust Auto-Nonvolatile Schmitt Trigger-Based Latch Design Using Ferroelectric CNTFET Technology. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 2022, 69, 1829-1840.	1.7	3
125	A Learning Based Contrast Specific no Reference Image Quality Assessment Algorithm. , 2022, , .		3
126	Design and Evaluating Carbon Nanotube Interconnects for a Generic Delta MIN. , 2011, , .		2

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127	Low-voltage multi-V<inf>TH</inf> single-supply level converters based on CNTFETs. , 2014, , .		2
128	Robust Carbon Nanotube Field Effect Transistor-Based Penternary Logic Circuits. Journal of Computational and Theoretical Nanoscience, 2014, 11, 2055-2062.	0.4	2
129	Islanding detection of solar power plants by considering the dynamics of PV and MPPT. , 2014, , .		2
130	A Comparative Performance Analysis of Copper and MWCNT Bundle Interconnects in Ternary Logic. , 2018, , .		2
131	An Energy-Efficient Crosstalk Reduction Strategy for On-Chip Buses Using Carbon-Based Transistors and Interconnects. ECS Journal of Solid State Science and Technology, 2021, 10, 051006.	0.9	2
132	An ultra-efficient recycling folded cascode OTA based on GAA-CNTFET technology for MEMS/NEMS capacitive readout applications. AEU - International Journal of Electronics and Communications, 2021, 136, 153773.	1.7	2
133	Crosstalk Delay and Noise Optimization in Nanoscale Multi-line Interconnects Based on Repeater Staggering in Ternary Logic. ECS Journal of Solid State Science and Technology, 2021, 10, 101003.	0.9	2
134	On the Design of Multi-Valued Multi-Phase Clock Generators Based on Carbon Nanotube FETs. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 314-318.	0.1	2
135	A Magnetic Reconfigurable Ternary NOR/NAND Logic for Logic-in-Memory Applications. Spin, 0, , .	0.6	2
136	An Efficient CNTFET Based 7-Input Minority Gate. International Journal of VLSI Design & Communication Systems, 2013, 4, 1-9.	0.2	1
137	Investigating Active Shielding Method for Reducing the Crosstalk Effects in Copper and MWCNT Bundle Interconnects in Ternary Logic. , 2018, , .		1
138	Fast and energy-efficient FPGA realization of RNS reverse converter for the ternary 3-moduli set {3nâ€“2, 3nâ€“1, 3n}. SN Applied Sciences, 2020, 2, 1.	1.5	1
139	Energy efficient hybrid full adder design for digital signal processing in nanoelectronics. Analog Integrated Circuits and Signal Processing, 2021, 109, 135-151.	0.9	1
140	High-Accuracy Spintronic Approximate Compressors for Error-Resilient In-Memory Computing. Spin, 2022, 12, .	0.6	1
141	A low-power voltage level converter for energy-efficient nanoelectronic circuits. International Journal of Circuits and Architecture Design, 2015, 1, 343.	0.1	0
142	An ultra-energy-efficient crosstalk-immune interconnect architecture based on multilayer graphene nanoribbons for deep-nanometer technologies. Journal of Computational Electronics, 2021, 20, 1411-1421.	1.3	0
143	Adiabatic 4:2 Compressors Based on 10-nm Gate-All-Around CNTFET for Low-Power Computing. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 1222-1234.	0.1	0