Luigi Raffo

List of Publications by Year
in descending order

178 papers	2,051 citations	361413 20 h-index	377865 34 g-index
182 all docs	182 docs citations	182 times ranked	1903 citing authors

#	Article	IF	Citations
1	An Adaptive Cognitive Sensor Node for ECG Monitoring in the Internet of Medical Things. IEEE Access, 2022, 10, 1688-1705.	4.2	14
2	Target-Aware Neural Architecture Search and Deployment for Keyword Spotting. IEEE Access, 2022, 10, 40687-40700.	4.2	2
3	The Multi-Dataflow Composer tool: An open-source tool suite for optimized coarse-grain reconfigurable hardware accelerators and platform design. Microprocessors and Microsystems, 2021, 80, 103326.	2.8	6
4	ALOHA: A Unified Platform-Aware Evaluation Method for CNNs Execution on Heterogeneous Systems at the Edge. IEEE Access, 2021, 9, 133289-133308.	4.2	7
5	Mutual Impact between Clock Gating and High Level Synthesis in Reconfigurable Hardware Accelerators. Electronics (Switzerland), 2021, 10, 73.	3.1	3
6	A non-invasive multimodal foetal ECGâ€"Doppler dataset for antenatal cardiology research. Scientific Data, 2021, 8, 30.	5.3	9
7	Impact of pulsed-wave-Doppler velocity-envelope tracing techniques on classification of complete fetal cardiac cycles. PLoS ONE, 2021, 16, e0248114.	2.5	2
8	Runtime Adaptive IoMT Node on Multi-Core Processor Platform. Electronics (Switzerland), 2021, 10, 2572.	3.1	2
9	Design and Usability Assessment of a Multi-Device SOA-Based Telecare Framework for the Elderly. IEEE Journal of Biomedical and Health Informatics, 2020, 24, 268-279.	6.3	35
10	Optimizing Temporal Convolutional Network Inference on FPGA-Based Accelerators. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 348-361.	3.6	21
11	Annotated real and synthetic datasets for non-invasive foetal electrocardiography post-processing benchmarking. Data in Brief, 2020, 33, 106399.	1.0	3
12	Feasibility Study and Porting of the Damped Least Square Algorithm on FPGA. IEEE Access, 2020, 8, 175483-175500.	4.2	1
13	ZyON: Enabling Spike Sorting on APSoC-Based Signal Processors for High-Density Microelectrode Arrays. IEEE Access, 2020, 8, 218145-218160.	4.2	5
14	Wavelet denoising as a post-processing enhancement method for non-invasive foetal electrocardiography. Computer Methods and Programs in Biomedicine, 2020, 195, 105558.	4.7	25
15	Automatic detection of complete and measurable cardiac cycles in antenatal pulsed-wave Doppler signals. Computer Methods and Programs in Biomedicine, 2020, 190, 105336.	4.7	11
16	Morphological Neural Computation Restores Discrimination of Naturalistic Textures in Trans-radial Amputees. Scientific Reports, 2020, 10, 527.	3.3	30
17	Systematic analysis of wavelet denoising methods for neural signal processing. Journal of Neural Engineering, 2020, 17, 066016.	3.5	17
18	NeuPow. ACM Transactions on Design Automation of Electronic Systems, 2020, 25, 1-29.	2.6	6

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19	Systematic analysis of single- and multi-reference adaptive filters for non-invasive fetal electrocardiography. Mathematical Biosciences and Engineering, 2020, 17, 286-308.	1.9	11
20	Hardware/Software Self-adaptation in CPS: The CERBERO Project Approach. Lecture Notes in Computer Science, 2019, , 416-428.	1.3	4
21	CERBERO: Cross-layer modEl-based fRamework for multi-oBjective dEsign of reconfigurable systems in unceRtain hybRid envirOnments. , 2019, , .		4
22	NeuPow. , 2019, , .		4
23	Reconfigurable Adaptive Multiple Transform Hardware Solutions for Versatile Video Coding. IEEE Access, 2019, 7, 153258-153268.	4.2	1
24	A runtime-adaptive cognitive IoT node for healthcare monitoring. , 2019, , .		10
25	Comparison of Single- and Multi-reference QRD-RLS adaptive filter for non-invasive fetal electrocardiography. , 2019, 2019, 1-5.		1
26	Sixâ€Month Assessment of a Hand Prosthesis with Intraneural Tactile Feedback. Annals of Neurology, 2019, 85, 137-154.	5.3	140
27	An integrated hardware/software design methodology for signal processing systems. Journal of Systems Architecture, 2019, 93, 1-19.	4.3	18
28	Dataflow-Functional High-Level Synthesis for Coarse-Grained Reconfigurable Accelerators. IEEE Embedded Systems Letters, 2019, 11, 69-72.	1.9	6
29	Challenging CPS Trade-off Adaptivity with Coarse-Grained Reconfiguration. Lecture Notes in Electrical Engineering, 2019, , 57-63.	0.4	2
30	Objective Human Gustatory Sensitivity Assessment Through a Portable Electronic Device. , 2018, , .		0
31	Multi-Grain Reconfiguration for Advanced Adaptivity in Cyber-Physical Systems. , 2018, , .		3
32	NEURA <scp>ghe</scp>. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-24.	2.5	50
33	Functional estimation of bony segment lengths using magneto-inertial sensing: Application to the humerus. PLoS ONE, 2018, 13, e0203861.	2.5	7
34	Exploiting All Programmable SoCs in Neural Signal Analysis: A Closed-Loop Control for Large-Scale CMOS Multielectrode Arrays. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 839-850.	4.0	17
35	Home tele-rehabilitation for rheumatic patients: impact and satisfaction of care analysis. Journal of Telemedicine and Telecare, 2017, 23, 292-300.	2.7	17
36	Challenging the Best HEVC Fractional Pixel FPGA Interpolators With Reconfigurable and Multifrequency Approximate Computing. IEEE Embedded Systems Letters, 2017, 9, 65-68.	1.9	15

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37	In vivo estimation of the shoulder joint center of rotation using magneto-inertial sensors: MRI-based accuracy and repeatability assessment. BioMedical Engineering OnLine, 2017, 16, 34.	2.7	31
38	A Novel Embedded System for Direct, Programmable Stimulation of the Peripheral Neural System. , 2017, , .		0
39	A closed-loop system for neural networks analysis through high density MEAs. , 2017, , .		0
40	Feasibility study of real-time spiking neural network simulations on a swarm intelligence based digital architecture. , 2017, , .		1
41	Hardware design methodology using lightweight dataflow and its integration with low power techniques. Journal of Systems Architecture, 2017, 78, 15-29.	4.3	5
42	On-FPGA real-time processing of biological signals from high-density MEAs: a design space exploration. , 2017, , .		5
43	A Precision Pseudo Resistor Bias Scheme for the Design of Very Large Time Constant Filters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 762-766.	3.0	34
44	Real-Time neural signal decoding on heterogeneous MPSocs based on VLIW ASIPs. Journal of Systems Architecture, 2017, 76, 89-101.	4.3	2
45	Comparative evaluation of different wavelet thresholding methods for neural signal processing. , 2017, 2017, 1042-1045.		4
46	A 64-channels neural interface for biopotentials recording and PNS stimulation. , 2017, 2017, 1938-1941.		1
47	EARNEST: A 64 channel device for neural recording and sensory touch restoration in neural prosthetics. , 2017, , .		2
48	An FPGA Platform for Real-Time Simulation of Spiking Neuronal Networks. Frontiers in Neuroscience, 2017, 11, 90.	2.8	69
49	An automated system for the objective evaluation of human gustatory sensitivity using tongue biopotential recordings. PLoS ONE, 2017, 12, e0177246.	2.5	11
50	Modelling and Automated Implementation of Optimal Power Saving Strategies in Coarse-Grained Reconfigurable Architectures. Journal of Electrical and Computer Engineering, 2016, 2016, 1-27.	0.9	3
51	The HEREiAM Tele-social-care Platform for Collaborative Management of Independent Living. , 2016, , .		7
52	Demo: Reconfigurable Platform Composer Tool. , 2016, , .		0
53	A high-efficiency runtime reconfigurable IP for CNN acceleration on a mid-range all-programmable SoC. , 2016, , .		18
54	Coarse grain reconfiguration: Power estimation and management flow for hybrid gated systems. , 2016, , .		0

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55	Low power design methodology for signal processing systems using lightweight dataflow techniques. , 2016, , .		1
56	Dataflow-Based Design of Coarse-Grained Reconfigurable Platforms. , 2016, , .		2
57	Investigation on the hermeticity of an implantable package with 32 feedthroughs for neural prosthetic applications. , 2016, 2016, 1967-1970.		4
58	A Custom dual-processor System for Real-time Neural Signal Processing. IFAC-PapersOnLine, 2016, 49, 61-67.	0.9	0
59	Runtime Energy versus Quality Tuning in Motion Compensation Filters for HEVC. IFAC-PapersOnLine, 2016, 49, 145-152.	0.9	5
60	An integrated interface for peripheral neural system recording and stimulation: system design, electrical tests and in-vivo results. Biomedical Microdevices, 2016, 18, 35.	2.8	14
61	Real-Time Neural Signals Decoding onto Off-the-Shelf DSP Processors for Neuroprosthetic Applications. IEEE Transactions on Neural Systems and Rehabilitation Engineering, 2016, 24, 993-1002.	4.9	14
62	On-the-fly adaptivity for process networks over shared-memory platforms. Microprocessors and Microsystems, 2016, 46, 240-254.	2.8	3
63	Curbing the roofline. , 2016, , .		12
64	Estimation of the center of rotation using wearable magneto-inertial sensors. Journal of Biomechanics, 2016, 49, 3928-3933.	2.1	19
65	Adaptable AES implementation with power-gating support. , 2016, , .		3
66	Automated Design Flow for Multi-Functional Dataflow-Based Platforms. Journal of Signal Processing Systems, 2016, 85, 143-165.	2.1	14
67	Power and clock gating modelling in coarse grained reconfigurable systems. , 2016, , .		8
68	MPSoCs for real-time neural signal decoding: A low-power ASIP-based implementation. Microprocessors and Microsystems, 2016, 43, 67-80.	2.8	4
69	Early Stage Automatic Strategy for Power-Aware Signal Processing Systems Design. Journal of Signal Processing Systems, 2016, 82, 311-329.	2.1	0
70	Power modelling for saving strategies in coarse grained reconfigurable systems. , 2015, , .		1
71	Exploring custom heterogeneous MPSoCs for real-time neural signal decoding. , 2015, , .		2
72	The challenge of collaborative telerehabilitation: conception and evaluation of a telehealth system enhancement for home‑therapy follow‑up. Concurrency Computation Practice and Experience, 2015, 27, 2889-2906.	2.2	3

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73	Coarse‑grained reconfiguration: dataflow‑based power management. IET Computers and Digital Techniques, 2015, 9, 36-48.	1.2	12
74	Reconfigurable coprocessors synthesis in the MPEG-RVC domain. , 2015, , .		8
75	Computing Swarms for Self-Adaptiveness and Self-Organization in Floating-Point Array Processing. ACM Transactions on Autonomous and Adaptive Systems, 2015, 10, 1-34.	0.8	1
76	An HV-CMOS Integrated Circuit for Neural Stimulation in Prosthetic Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 184-188.	3.0	27
77	Toward the Development of a Neuro-Controlled Bidirectional Hand Prosthesis. Lecture Notes in Computer Science, 2015, , 105-110.	1.3	0
78	Automated power gating methodology for dataflow-based reconfigurable systems. , 2015, , .		6
79	A configurable biopotentials acquisition module suitable for fetal electrocardiography studies. , 2015, , .		0
80	Home telemonitoring of vital signs through a TV-based application for elderly patients. , 2015, , .		12
81	Impact of Threshold Computation Methods in Hardware Wavelet Denoising Implementations for Neural Signal Processing. Communications in Computer and Information Science, 2015, , 66-81.	0.5	2
82	Real-time blind audio source separation: performance assessment on an advanced digital signal processor. Journal of Supercomputing, 2014, 70, 1555-1576.	3.6	6
83	Power-awarness in coarse-grained reconfigurable designs: A dataflow based strategy. , 2014, , .		3
84	Tactile sensors with integrated piezoelectric polymer and low voltage organic thin-film transistors. , 2014, , .		7
85	A Temperature Transducer Based on a Low-Voltage Organic Thin-Film Transistor Detecting Pyroelectric Effect. IEEE Electron Device Letters, 2014, 35, 1296-1298.	3.9	20
86	An advanced algorithm for fetal heart rate estimation from non-invasive low electrode density recordings. Physiological Measurement, 2014, 35, 1621-1636.	2.1	29
87	The multi-dataflow composer tool: generation of on-the-fly reconfigurable platforms. Journal of Real-Time Image Processing, 2014, 9, 233-249.	3.5	21
88	A Device for Local or Remote Monitoring of Hand Rehabilitation Sessions for Rheumatic Patients. IEEE Journal of Translational Engineering in Health and Medicine, 2014, 2, 1-11.	3.7	19
89	Telemedicine Applied to Kinesiotherapy for Hand Dysfunction in Patients with Systemic Sclerosis and Rheumatoid Arthritis: Recovery of Movement and Telemonitoring Technology. Journal of Rheumatology, 2014, 41, 1324-1333.	2.0	39
90	Online process transformation for polyhedral process networks in shared-memory MPSoCs. , 2014, , .		0

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91	High performance, foldable, organic memories based on ultra-low voltage, thin film transistors. Organic Electronics, 2014, 15, 3595-3600.	2.6	18
92	A Custom MPSoC Architecture With Integrated Power Management for Real-Time Neural Signal Decoding. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 230-241.	3.6	8
93	Automated design flow for coarse-grained reconfigurable platforms: An RVC-CAL multi-standard decoder use-case. , 2014, , .		11
94	A Stream Buffer Mechanism for Pervasive Splitting Transformations on Polyhedral Process Networks. , 2014, , .		1
95	ASAM: Automatic architecture synthesis and application mapping. Microprocessors and Microsystems, 2013, 37, 1002-1019.	2.8	23
96	A system-level approach to adaptivity and fault-tolerance in NoC-based MPSoCs: The MADNESS project. Microprocessors and Microsystems, 2013, 37, 515-529.	2.8	13
97	Behavioural models for analog to digital conversion architectures for deep submicron technology nodes. , 2013, , .		1
98	Exploring hardware support for scaling irregular applications on multi-node multi-core architectures. , 2013, , .		1
99	DSE and profiling of multi-context coarse-grained reconfigurable systems. , 2013, , .		13
100	A collaborative approach to the telerehabilitation of patients with hand impairments. , 2013, , .		2
101	A coarse-grained reconfigurable approach for low-power spike sorting architectures. , 2013, , .		13
102	NInFEA: an embedded framework for the real-time evaluation of fetal ECG extraction algorithms. Biomedizinische Technik, 2013, 58, 13-26.	0.8	10
103	An Integrated Portable Device for the Hand Functional Assessment in the Clinical Practice. Communications in Computer and Information Science, 2013, , 97-110.	0.5	0
104	Concurrent hybrid switching for massively parallel systems-on-chip. , 2012, , .		3
105	System Adaptivity and Fault-Tolerance in NoC-based MPSoCs: The MADNESS Project Approach. , 2012, , .		22
106	Multi-purpose systems: A novel dataflow-based generation and mapping strategy. , 2012, , .		7
107	Exploiting binary translation for fast ASIP design space exploration on FPGAs. , 2012, , .		2
108	Combining on-hardware prototyping and high-level simulation for DSE of multi-ASIP systems. , 2012, , .		1

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109	ASAM: Automatic Architecture Synthesis and Application Mapping. , 2012, , .		8
110	A sigma-delta architecture for recording of peripheral neural signals in prosthetic applications. , 2012, , .		3
111	Enabling Fast ASIP Design Space Exploration: An FPGA-Based Runtime Reconfigurable Prototyper. VLSI Design, 2012, 2012, 1-16.	0.5	10
112	A PORTABLE REAL-TIME MONITORING SYSTEM FOR KINESITHERAPIC HAND REHABILITATION EXERCISES. , 2012, , .		1
113	KeepInTouch: A telehealth system to improve the follow-up of chronic patients. , 2011, , .		11
114	The Multi-Dataflow Composer tool: A runtime reconfigurable HDL platform composer. , 2011, , .		13
115	Real-time processing of tfLIFE neural signals on embedded DSP platforms: A case study. , 2011, , .		8
116	Peripheral Neural Activity Recording and Stimulation System. IEEE Transactions on Biomedical Circuits and Systems, 2011, 5, 368-379.	4.0	35
117	Towards self-adaptive networks on chip for massively parallel processors. , 2011, , .		0
118	A fast MPI-based parallel framework for cycle-accurate HDL multi-parametric simulations. International Journal of High Performance Systems Architecture, 2010, 2, 187.	0.3	6
119	Exploiting FPGAs for technology-aware system-level evaluation of multi-core architectures. , 2010, , .		2
120	Self-coordinated On-Chip Parallel Computing: A Swarm Intelligence Approach. Studies in Computational Intelligence, 2010, , 91-112.	0.9	3
121	Self organization on a swarm computing fabric. , 2010, , .		2
122	Enabling fast Network-on-Chip topology selection: an FPGA-based runtime reconfigurable prototyper. , 2010, , .		1
123	An FPGA-Based Framework for Technology-Aware Prototyping of Multicore Embedded Architectures. IEEE Embedded Systems Letters, 2010, 2, 5-9.	1.9	16
124	Impact of Half-Duplex and Full-Duplex DMA Implementations on NoC Performance. , 2010, , .		1
125	A sleep apnoea keeper in a wearable device for Continuous detection and screening during daily life. , 2008, , .		8
126	A pervasive telemedicine system exploiting the DVB-T technology. , 2008, , .		3

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127	A Network on Chip Architecture for Heterogeneous Traffic Support with Non-Exclusive Dual-Mode Switching. , 2008, , .		1
128	A DVB-T framework for the remote monitoring of cardiopathic and diabetic patients. , 2008, , .		2
129	A DSP algorithm and system for real-time fetal ECG extraction. , 2008, , .		7
130	A Novel Non-exclusive Dual-Mode Architecture for MPSoCs-Oriented Network on Chip Designs. Lecture Notes in Computer Science, 2008, , 96-105.	1.3	5
131	A Surface Tension and Coalescence Model for Dynamic Distributed Resources Allocation in Massively Parallel Processors on-Chip. Studies in Computational Intelligence, 2008, , 335-345.	0.9	5
132	A Tele-home Care System Exploiting the DVB-T Technology and MHP. Methods of Information in Medicine, 2008, 47, 223-224.	1.2	14
133	Designing Routing and Message-Dependent Deadlock Free Networks on Chips. , 2008, , 337-355.		2
134	Real-time foetal ECG extraction with JADE on floating point DSP. Electronics Letters, 2007, 43, 963.	1.0	10
135	Synthesis of Predictable Networks-on-Chip-Based Interconnect Architectures for Chip Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 869-880.	3.1	35
136	NoC Design and Implementation in 65nm Technology. , 2007, , .		51
137	A Layout-Aware Analysis of Networks-on-Chip and Traditional Interconnects for MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 421-434.	2.7	47
138	Optimizing the serialization factor in Networks-on-Chip: a case of study. , 2007, , .		0
139	On the impact of serialization on the cache performances in Network-on-Chip based MPSoCs. , 2007, , .		1
140	Area and Power Modeling for Networks-on-Chip with Layout Awareness. VLSI Design, 2007, 2007, 1-12.	0.5	22
141	Automatic Application Partitioning on FPGA/CPU Systems Based on Detailed Low-Level Information. , 2006, , .		1
142	Designing Message-Dependent Deadlock Free Networks on Chips for Application-Specific Systems on Chips. , 2006, , .		21
143	Routing Aware Switch Hardware Customization for Networks on Chips. , 2006, , .		6
144	Designing Application-Specific Networks on Chips with Floorplan Information. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	26

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145	A CMOS, fully integrated sensor for electronic detection of DNA hybridization. IEEE Electron Device Letters, 2006, 27, 595-597.	3.9	57
146	Reconfigurable Coprocessor for Multimedia Application Domain. Journal of Signal Processing Systems, 2006, 44, 135-152.	1.0	16
147	Fully electronic DNA hybridization detection by a standard CMOS biochip. Sensors and Actuators B: Chemical, 2006, 118, 41-46.	7.8	41
148	Stigmergic approaches applied to flexible fault-tolerant digital VLSI architectures. Journal of Parallel and Distributed Computing, 2006, 66, 1014-1024.	4.1	8
149	A charge-modulated FET for detection of biomolecular processes: conception, modeling, and simulation. IEEE Transactions on Electron Devices, 2006, 53, 158-166.	3.0	144
150	Area and Power Modeling Methodologies for Networks-on-Chip. , 2006, , .		9
151	Cooperative VLSI Tiled Architectures: Stigmergy in a Swarm Coprocessor. Lecture Notes in Computer Science, 2006, , 396-403.	1.3	4
152	A Low-Power Integrated Smart Sensor with on-Chip Real-Time Image Processing Capabilities. Eurasip Journal on Advances in Signal Processing, 2005, 2005, 1.	1.7	2
153	A VLSI Multiplication-and-Add Scheme Based on Swarm Intelligence Approaches. Lecture Notes in Computer Science, 2004, , 13-24.	1.3	3
154	A Swarm Intelligence Based VLSI Multiplication-and-Add Scheme. Lecture Notes in Computer Science, 2004, , 362-371.	1.3	1
155	44.6% processing cycles reduction in GSM voice coding by low-power reconfigurable co-processor architecture. Electronics Letters, 2002, 38, 1524.	1.0	3
156	Analogue VLSI primitives for perceptual tasks in machine vision. Neural Computing and Applications, 1998, 7, 216-228.	5.6	5
157	Analog computation for phase-based disparity estimation: continuous and discrete models. Machine Vision and Applications, 1998, 11, 83-95.	2.7	8
158	Analysis and synthesis of double-layer MOSFET networks for smart sensory systems. Electronics Letters, 1998, 34, 1903.	1.0	0
159	Analog VLSI circuits as physical structures for perception in early visual tasks. IEEE Transactions on Neural Networks, 1998, 9, 1483-1494.	4.2	25
160	Functional Periodic Intracortical Couplings Induced by Structured Lateral Inhibition in a Linear Cortical Network. Neural Computation, 1997, 9, 525-531.	2.2	4
161	Design of an ASIP architecture for low-level visual elaborations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1997, 5, 145-153.	3.1	10
162	A recurrent neural architecture mimicking cortical preattentive vision systems. Neurocomputing, 1996, 11, 155-170.	5.9	4

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163	A programmable VLSI architecture based on multilayer CNN paradigms for real-time visual processing. International Journal of Circuit Theory and Applications, 1996, 24, 357-367.	2.0	3
164	A VLSI Image Processing Architecture Dedicated to Real-Time Quality Control Analysis in an Industrial Plant. Real Time Imaging, 1996, 2, 361-371.	1.6	0
165	Analysis and synthesis of resistive networks for distributed visual elaborations. Electronics Letters, 1996, 32, 743.	1.0	11
166	Resistive network implementing maps of Gabor functions of any phase. Electronics Letters, 1995, 31, 1913-1914.	1.0	15
167	Adaptive resistive network for stereo depth estimation. Electronics Letters, 1995, 31, 1909-1910.	1.0	1
168	A neuromorphic architecture for cortical multilayer integration of early visual tasks. Machine Vision and Applications, 1995, 8, 305-314.	2.7	1
169	A neuromorphic architecture for cortical multilayer integration of early visual tasks. Machine Vision and Applications, 1995, 8, 305-314.	2.7	6
170	A Multi-Layer Analog VLSI Architecture for Texture Analysis Isomorphic to Cortical Cells in Mammalian Visual System. , 1994, , 61-70.		0
171	Artificial visual orientation map implemented as an inhomogeneous active resistor mesh. Electronics Letters, 1993, 29, 963-964.	1.0	4
172	Neural clustering algorithms for classification and pre-placement of VLSI cells. , 0, , .		1
173	A distributed adaptive architecture for analog stereo depth estimation. , 0, , .		1
174	Processing time saving in low power voice coding applications using synchronous reconfigurable co-processing architecture. , 0, , .		1
175	Run-time Adaptive Resources Allocation and Balancing on Nanoprocessors Arrays. , 0, , .		2
176	×pipes Lite: A Synthesis Oriented Design Library For Networks on Chips. , 0, , .		97
177	Fetal Pulsed-Wave Doppler Atrioventricular Activity Detection by Envelope Extraction and Processing. , 0, , .		2
178	A micro-power mixed signal IC for battery-operated burglar alarm systems. , 0, , .		2