

Rainer Doemer

List of Publications by Year in descending order

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59
papers

903
citations

1039406

9
h-index

887659

17
g-index

60
all docs

60
docs citations

60
times ranked

227
citing authors

#	ARTICLE	IF	CITATIONS
1	SPECC: Specification Language and Methodology. , 2000, , .		423
2	System-on-Chip Environment: A SpecC-Based Framework for Heterogeneous MPSoC Design. Eurasip Journal on Embedded Systems, 2008, 2008, 647953.	1.2	84
3	Result-Oriented Modeling – A Novel Technique for Fast and Accurate TLM. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1688-1699.	1.9	30
4	Abstract, Multifaceted Modeling of Embedded Processors for System Level Design. , 2007, , .		29
5	Automatic Layer-Based Generation of System-On-Chip Bus Communication Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1676-1687.	1.9	26
6	Fast and accurate processor models for efficient MPSoC design. ACM Transactions on Design Automation of Electronic Systems, 2010, 15, 1-26.	1.9	25
7	Quantitative analysis of the speed/accuracy trade-off in transaction level modeling. Transactions on Embedded Computing Systems, 2008, 8, 1-29.	2.1	23
8	Out-of-Order Parallel Discrete Event Simulation for Transaction Level Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1859-1872.	1.9	21
9	System-level communication modeling for network-on-chip synthesis. , 2005, , .		18
10	Exploiting Thread and Data Level Parallelism for Ultimate Parallel SystemC Simulation. , 2017, , .		17
11	Code and Data Structure Partitioning for Parallel and Flexible MPSoC Specification Using Designer-Controlled Recoding. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1078-1090.	1.9	15
12	Multicore Simulation of Transaction-Level Models Using the SoC Environment. IEEE Design and Test of Computers, 2011, 28, 20-31.	1.4	14
13	Multi-core parallel simulation of System-level Description Languages. , 2011, , .		13
14	An Interactive Design Environment for C-Based High-Level Synthesis of RTL Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 466-475.	2.1	12
15	Automatic generation of hardware dependent software for MPSoCs from abstract system specifications. , 2008, , .		12
16	Introducing Preemptive Scheduling in Abstract RTOS Models using Result Oriented Modeling. , 2008, , .		11
17	Optimizing thread-to-core mapping on manycore platforms with distributed Tag Directories. , 2015, , .		10
18	Fast and Accurate Transaction Level Models using Result Oriented Modeling. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	9

#	ARTICLE	IF	CITATIONS
19	Parallel discrete event simulation of Transaction Level Models. , 2012, , .		9
20	Seven Obstacles in the Way of Standard-Compliant Parallel SystemC Simulation. IEEE Embedded Systems Letters, 2016, 8, 81-84.	1.3	9
21	Automatic network generation for system-on-chip communication design. , 2005, , .		8
22	Optimized Out-of-Order Parallel Discrete Event Simulation Using Predictions. , 2013, , .		8
23	Automated estimation of power consumption for rapid system level design. , 2014, , .		6
24	Creating Explicit Communication in SoC Models Using Interactive Re-Coding. , 2007, , .		5
25	System-level development of embedded software. , 2010, , .		5
26	Advances in Parallel Discrete Event Simulation for Electronic System-Level Design. IEEE Design and Test, 2013, 30, 45-54.	1.1	5
27	ESL design and multi-core validation using the System-on-Chip Environment. , 2010, , .		4
28	Computer-Aided Recoding to Create Structured and Analyzable System Models. Transactions on Embedded Computing Systems, 2012, 11S, 1-27.	2.1	4
29	An optimizing compiler for out-of-order parallel ESL simulation exploiting instance isolation. , 2012, , .		4
30	Port call path sensitive conflict analysis for instance-aware parallel SystemC simulation. , 2018, , .		4
31	May-happen-in-parallel analysis based on segment graphs for safe ESL models. , 2014, , .		4
32	Eliminating race conditions in system-level models by using parallel simulation infrastructure. , 2012, , .		3
33	Powermonitor: a versatile API for automated power-aware ESL design. , 2014, , .		3
34	May-happen-in-parallel analysis based on segment graphs for safe ESL models. , 2014, , .		3
35	AUTOMATIC GENERATION OF COMMUNICATION ARCHITECTURES. , 2005, , 179-188.		3
36	Automatic re-coding of reference code into structured and analyzable SoC models. , 2008, , .		2

#	ARTICLE	IF	CITATIONS
37	May-Happen-in-Parallel Analysis of ESL Models using UPPAAL Model Checking. , 2015, , .		2
38	Hybrid analysis of SystemC models for fast and accurate parallel simulation. , 2017, , .		2
39	ConcurrenC: A New Approach towards Effective Abstraction of C-Based SLDLs. IFIP Advances in Information and Communication Technology, 2009, , 57-65.	0.5	2
40	Parallel Simulation. , 2016, , 1-32.		2
41	Analyzing Variable Entanglement for Parallel Simulation of SystemC TLM-2.0 Models. Transactions on Embedded Computing Systems, 2019, 18, 1-20.	2.1	2
42	SOFTWARE AND DRIVER SYNTHESIS FROM TRANSACTION LEVEL MODELS. , 2005, , 65-76.		2
43	Programming MPSoC platforms: Road works ahead!. , 2009, , .		1
44	Computer-aided recoding for multi-core systems. , 2010, , .		1
45	Out-of-order parallel simulation for ESL design. , 2012, , .		1
46	A program state machine based virtual processing model in SystemC. ACM SIGBED Review, 2015, 11, 7-12.	1.8	1
47	Parallel Simulation. , 2017, , 533-564.		1
48	Event Delivery using Prediction for Faster Parallel SystemC Simulation. , 2020, , .		1
49	Scaled Static Analysis and IP Reuse for Out-of-Order Parallel SystemC Simulation. International Journal of Parallel Programming, 2021, 49, 200-215.	1.1	1
50	Improving Parallelism in System Level Models by Assessing PDES Performance. , 2021, , .		1
51	Designer-Controlled Generation of Parallel and Flexible Heterogeneous MPSoC Specification. Proceedings - Design Automation Conference, 2007, , .	0.0	1
52	An Interactive Design Environment for C-based High-Level Synthesis. , 2007, , 135-144.		1
53	A fast heuristic scheduling algorithm for periodic ConcurrenC models. , 2010, , .		0
54	Communication protocol analysis of transaction-level models using Satisfiability Modulo Theories. , 2015, , .		0

#	ARTICLE	IF	CITATIONS
55	Efficient Modeling of Embedded Systems Using Computer-Aided Recoding. IFIP Advances in Information and Communication Technology, 2009, , 310-311.	0.5	0
56	SCE: System-on-Chip Environment. , 2016, , 1-32.		0
57	SCE: System-on-Chip Environment. , 2017, , 1019-1050.		0
58	Pushing the Limits of Parallel Discrete Event Simulation for SystemC. , 2021, , 97-105.		0
59	Embedded Software Development in a System-Level Design Flow. , 2007, , 289-298.		0