Hong-Yun Kim

List of Publications by Year in Descending Order

101 papers	1,174 citations	15 h-index	30 g-index
123 ext. papers	1,529 ext. citations	3.4 avg, IF	4.49 L-index

#	Paper	IF	Citations
101	Energy-Efficient CNN Personalized Training by Adaptive Data Reformation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2022**, 1-1	2.5	
100	A Framework for Accelerating Transformer-based Language Model on ReRAM-based Architecture. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
99	Amnesiac DRAM: A Proactive Defense Mechanism Against Cold Boot Attacks. *IEEE Transactions on Computers*, **2021**, 70, 539-551	2.5	2
98	Quantization-Error-Robust Deep Neural Network for Embedded Accelerators. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	
97	Rare Computing: Removing Redundant Multiplications from Sparse and Repetitive Data in Deep Neural Networks. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	
96	Enabling the Large-Scale Emulation of Internet of Things Firmware With Heuristic Workarounds. *IEEE Security and Privacy*, **2021**, 2-11	2	
95	A Deep Neural Network Training Architecture with Inference-aware Heterogeneous Data-type. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	2
94	S-FLASH: A NAND Flash-based Deep Neural Network Accelerator Exploiting Bit-level Sparsity. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	1
93	CREMON: Cryptography Embedded on the Convolutional Neural Network Accelerator. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3337-3341	3.5	2
92	A Pragmatic Approach to On-device Incremental Learning System with Selective Weight Updates **2020**,		3
91	An Energy-Efficient Deep Convolutional Neural Network Training Accelerator for In Situ Personalization on Smart Devices. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2691-2702	5.5	14
90	An Energy-Efficient Deep Convolutional Neural Network Inference Processor With Enhanced Output Stationary Dataflow in 65-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 87-100	2.6	17
89	NAND-Net: Minimizing Computational Complexity of In-Memory Processing for Binary Neural Networks **2019**,		16
88	DC-PCM: Mitigating PCM Write Disturbance with Low Performance Overhead by Using Detection Cells. *IEEE Transactions on Computers*, **2019**, 68, 1741-1754	2.5	3
87	An Optimized Design Technique of Low-bit Neural Network Training for Personalization on IoT Devices **2019**,		9
86	A 12 Gb/s 1.59 mW/Gb/s Input-Data-Jitter-Tolerant Injection-Type CDR With Super-Harmonic Injection-Locking in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1972-1976	3.5	2
85	eSRCNN: A Framework for Optimizing Super-Resolution Tasks on Diverse Embedded CNN Accelerators **2019**,		1

84	An Energy-efficient Processing-in-memory Architecture for Long Short Term Memory in Spin Orbit Torque MRAM **2019**,		2
83	Sparse-Insertion Write Cache to Mitigate Write Disturbance Errors in Phase Change Memory. *IEEE Transactions on Computers*, **2019**, 68, 752-764	2.5	2
82	A 0.9-V 12-Gb/s Two-FIR Tap Direct DFE With Feedback-Signal Common-Mode Control. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 724-728	2.6	4
81	Elaborate Refresh: A Fine Granularity Retention Management for Deep Submicron DRAMs. *IEEE Transactions on Computers*, **2018**, 67, 1403-1415	2.5	2
80	A 0.65-V, 11.2-Gb/s Power Noise Tolerant Source-Synchronous Injection-Locked Receiver With Direct DTLB DFE. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1564-1568	3.5	3
79	A 10-Gb/s Reference-Less Baud-Rate CDR for Low Power Consumption With the Direct Feedback Method. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1539-1543	3.5	1
78	TrainWare **2018**,		3
77	A 5-Gb/s Digital Clock and Data Recovery Circuit With Reduced DCO Supply Noise Sensitivity Utilizing Coupling Network. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 380-384	2.6	7
76	An Input Data and Power Noise Inducing Clock Jitter Tolerant Reference-Less Digital CDR for LCD Intra-Panel Interface. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2017**, 64, 823-835	3.9	11
75	Bank-Group Level Parallelism. *IEEE Transactions on Computers*, **2017**, 66, 1428-1434	2.5	1
74	Energy-Efficient Design of Processing Element for Convolutional Neural Network. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 1332-1336	3.5	20
73	In-DRAM Data Initialization. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 3251-3254	2.6	2
72	A Kernel Decomposition Architecture for Binary-weight Convolutional Neural Networks **2017**,		14
71	Refresh-Aware Write Recovery Memory Controller. *IEEE Transactions on Computers*, **2017**, 66, 688-701	2.5	1
70	SENIN: An energy-efficient sparse neuromorphic system with on-chip learning **2017**,		1
69	A 21-Gbit/s 1.63-pJ/bit Adaptive CTLE and One-Tap DFE With Single Loop Spectrum Balancing Method. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 789-793	2.6	18
68	DRAM-Latency Optimization Inspired by Relationship between Row-Access Time and Refresh Timing. *IEEE Transactions on Computers*, **2016**, 65, 3027-3040	2.5	8
67	A 21%-Jitter-Improved Self-Aligned Dividerless Injection-Locked PLL With a VCO Control Voltage Ripple-Compensated Phase Detector. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 733-737	3.5	3

66	A 10-Gb/s 0.71-pJ/bit Forwarded-Clock Receiver Tolerant to High-Frequency Jitter in 65-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2016**, 63, 264-268	3.5	5
65	Q-DRAM: Quick-Access DRAM with Decoupled Restoring from Row-Activation. *IEEE Transactions on Computers*, **2016**, 65, 2213-2227	2.5	4
64	Private Over-Threshold Aggregation Protocols over Distributed Datasets. *IEEE Transactions on Knowledge and Data Engineering*, **2016**, 28, 2467-2479	4.2	2
63	Multiple clone row DRAM **2015**,		24
62	Hijacking the Vuze BitTorrent network: all your hop are belong to us. *IET Information Security*, **2015**, 9, 203-208	1.4	2
61	Timing Attacks on Access Privacy in Information Centric Networks and Countermeasures. *IEEE Transactions on Dependable and Secure Computing*, **2015**, 12, 675-687	3.9	28
60	A 9.6 Gb/s 0.96 mW/Gb/s Forwarded Clock Receiver With High Jitter Tolerance Using Mixing Cell Integrated Injection-Locked Oscillator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2015**, 62, 2495-2503	3.9	4
59	A Vision Processor With a Unified Interest-Point Detection and Matching Hardware for Accelerating a Stereo-Matching Algorithm. *IEEE Transactions on Circuits and Systems for Video Technology*, **2015**, 1-1	6.4	3
58	A Forwarded Clock Receiver Based on Injection-Locked Oscillator With AC-Coupled Clock Multiplication Unit in $0.13~boldsymbol {mu } $ m CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 988-992	2.6	
57	An 11.5 Gb/s 1/4th Baud-Rate CTLE and Two-Tap DFE With Boosted High Frequency Gain in 110-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 588-592	2.6	6
56	A 9.6-Gb/s 1.22-mW/Gb/s Data-Jitter Mixing Forwarded-Clock Receiver in 65-nm CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2023-2033	2.6	4
55	Hybrid Temperature Sensor Network for Area-Efficient On-Chip Thermal Map Sensing. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 610-618	5.5	7
54	A Forwarded-Clock Receiver With Constant and Wide-Range Jitter-Tracking Bandwidth. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2014**, 61, 153-157	3.5	1
53	**2014**,		33
52	A Quarter-Rate Forwarded Clock Receiver Based on ILO With Low Jitter Tracking Bandwidth Variation Using Phase Shifting Phenomenon in 65 nm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 2482-2490	3.9	3
51	A 5 Gbps 1.6 mW/G bps/CH Adaptive Crosstalk Cancellation Scheme With Reference-less Digital Calibration and Switched Termination Resistors for Single-Ended Parallel Interface. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2014**, 61, 3016-3024	3.9	2
50	Secure Encounter-Based Mobile Social Networks: Requirements, Designs, and Tradeoffs. *IEEE Transactions on Dependable and Secure Computing*, **2013**, 10, 380-393	3.9	16
49	A Unified Graphics and Vision Processor With a 0.89 /spl mu/W/fps Pose Estimation Engine for Augmented Reality. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 206-216	2.6	13

48	A Reconfigurable SIMT Processor for Mobile Ray Tracing With Contention Reduction in Shared Memory. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2013**, 60, 938-950	3.9	9
47	A LOG-Induced SSN-Tolerant Transceiver for On-Chip Interconnects in COG-Packaged Source Driver IC for TFT-LCD. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 21-25	3.5	1
46	Peer Pressure: Exerting Malicious Influence on Routers at a Distance **2013**,		4
45	Computing energy-efficiency in the mobile GPU **2013**,		3
44	A 6.5-Gb/s 1-mW/Gb/s/CH Simple Capacitive Crosstalk Compensator in a 130-nm Process. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 302-306	3.5	1
43	PowerField: A Probabilistic Approach for Temperature-to-Power Conversion Based on Markov Random Field Theory. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* , **2013**, 32, 1509-1519	2.5	4
42	MRTP: Mobile Ray Tracing Processor With Reconfigurable Stream Multi-Processors for High Datapath Utilization. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 518-535	5.5	13
41	A 5.4-Gb/s Clock and Data Recovery Circuit Using Seamless Loop Transition Scheme With Minimal Phase Noise Degradation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2012**, 59, 2518-2528	3.9	5
40	An Adaptive Equalizer With the Capacitance Multiplication for DisplayPort Main Link in 0.18-mum CMOS. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 964-968	2.6	6
39	A 5.4/2.7/1.62-Gb/s Receiver for DisplayPort Version 1.2 With Multi-Rate Operation Scheme. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2012**, 59, 2858-2866	3.9	12
38	A Reconfigurable Heterogeneous Multimedia Processor for IC-Stacking on Si-Interposer. *IEEE Transactions on Circuits and Systems for Video Technology*, **2012**, 22, 589-604	6.4	4
37	A Mobile 3-D Display Processor With A Bandwidth-Saving Subdivider. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1082-1093	2.6	1
36	Homogeneous Stream Processors With Embedded Special Function Units for High-Utilization Programmable Shaders. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1691-1704	2.6	11
35	A Dual-Shader 3-D Graphics Processor With Fast 4-D Vector Inner Product Units and Power-Aware Texture Cache. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2011**, 19, 525-537	2.6	6
34	A Spread Spectrum Clock Generator for DisplayPort Main Link. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2011**, 58, 361-365	3.5	12
33	Area-efficient dynamic thermal management unit using MDLL with shared DLL scheme for many-core processors **2011**,		1
32	A 5.4 Gb/s clock and data recovery circuit using the seamless loop transition scheme without phase noise degradation **2011**,		2
31	An area efficient asynchronous gated ring oscillator TDC with minimum GRO stages **2010**,		2

30	A high resolution metastability-independent two-step gated ring oscillator TDC with enhanced noise shaping **2010**,		10
29	A Data-Pattern-Tolerant Adaptive Equalizer Using the Spectrum Balancing Method. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2010**, 57, 228-232	3.5	11
28	A 116 fps/74 mW Heterogeneous 3D-Media Processor for 3-D Display Applications. *IEEE Journal of Solid-State Circuits*, **2010**, 45, 652-667	5.5	8
27	A DLL With Jitter Reduction Techniques and Quadrature Phase Generation for DRAM Interfaces. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 1522-1530	5.5	11
26	A 5-Gb/s/pin Transceiver for DDR Memory Interface With a Crosstalk Suppression Scheme. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 2222-2232	5.5	4
25	A 0.13-mu m CMOS 6 Gb/s/pin Memory Transceiver Using Pseudo-Differential Signaling for Removing Common-Mode Noise Due to SSN. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 3146-3162	5.5	14
24	A 20 Gb/s 1:4 DEMUX Without Inductors and Low-Power Divide-by-2 Circuit in 0.13 $mu{hbox {m}}$ CMOS Technology. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 541-549	5.5	7
23	A 36 fps SXGA 3-D Display Processor Embedding a Programmable 3-D Graphics Rendering Engine. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 1247-1259	5.5	4
22	An Area Efficient Early ${Z}$ -Test Method for 3-D Graphics Rendering Hardware. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2008**, 55, 1929-1938	3.9	4
21	An Energy-Efficient Mobile Vertex Processor With Multithread Expanded VLIW Architecture and Vertex Caches. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 2257-2269	5.5	15
20	A low-power ROM using single charge-sharing capacitor and hierarchical bit line. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 313-322	2.6	6
19	A cost-effective VLSI architecture for anisotropic texture filtering in limited memory bandwidth. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2006**, 14, 254-267	2.6	0
18	An SoC with 1.3 gtexels/s 3-D graphics full pipeline for consumer applications. *IEEE Journal of Solid-State Circuits*, **2006**, 41, 71-84	5.5	23
17	A low-power SRAM using hierarchical bit line and local sense amplifiers. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 1366-1376	5.5	76
16	A 250-MHz-2-GHz wide-range delay-locked loop. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 1310-1321	5.5	33
15	A low-power CAM using pulsed NAND-NOR match-line and charge-recycling search-line driver. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 1736-1744	5.5	30
14	An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/a converter. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 761-774	5.5	49
13	A high-resolution synchronous mirror delay using successive approximation register. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 1997-2004	5.5	13

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12	A low-power ROM using charge recycling and charge sharing techniques. *IEEE Journal of Solid-State Circuits*, **2003**, 38, 641-653	5.5	20
11	A low-power charge-recycling ROM architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2003**, 11, 590-600	2.6	10
10	An advanced contrast enhancement using partially overlapped sub-block histogram equalization. *IEEE Transactions on Circuits and Systems for Video Technology*, **2001**, 11, 475-484	6.4	353
9	A hardware cost minimized fast Phong shader. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2001**, 9, 297-304	2.6	6
8	A real-time wavelet vector quantization algorithm and its VLSI architecture. *IEEE Transactions on Circuits and Systems for Video Technology*, **2000**, 10, 475-489	6.4	7
7	Comments on "New dynamic flip-flops for high-speed dual-modulus prescaler". *IEEE Journal of Solid-State Circuits*, **2000**, 35, 919-920	5.5	2
6	A new crosstalk compensation method in line inversion TFT-LCDs. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **1997**, 44, 552-555		8
5	A mode-changeable 2-D DCT/IDCT processor for digital VCR. *IEEE Transactions on Consumer Electronics*, **1996**, 42, 606-616	4.8	1
4	Buck converter with a new driving circuit in a TV power system. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **1996**, 43, 811-813		1
3	Adaptive selection of an index in a texture cache		2
2	A minimized hardware architecture of fast Phong shader using Taylor series approximation in 3D graphics		10
1	Semi-recursive VLSI architecture for two dimensional discrete wavelet transform		1