Hong-Yun Kim

List of Publications by Year
in descending order

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123	1,772	430442	344852
papers	citations	18 h-index	36 g-index

123	123	123	1326
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An advanced contrast enhancement using partially overlapped sub-block histogram equalization. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 475-484.	5.6	478
2	A low-power SRAM using hierarchical bit line and local sense amplifiers. IEEE Journal of Solid-State Circuits, 2005, 40, 1366-1376.	3.5	109
3	An 800-MHz low-power direct digital frequency synthesizer with an on-chip D/a converter. IEEE Journal of Solid-State Circuits, 2004, 39, 761-774.	3.5	71
4	A low-power CAM using pulsed NAND-NOR match-line and charge-recycling search-line driver. IEEE Journal of Solid-State Circuits, 2005, 40, 1736-1744.	3.5	48
5	NUAT: A non-uniform access time memory controller. , 2014, , .		44
6	An Energy-Efficient Deep Convolutional Neural Network Inference Processor With Enhanced Output Stationary Dataflow in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 87-100.	2.1	40
7	A 250-MHz-2-GHz wide-range delay-locked loop. IEEE Journal of Solid-State Circuits, 2005, 40, 1310-1321.	3.5	39
8	Timing Attacks on Access Privacy in Information Centric Networks and Countermeasures. IEEE Transactions on Dependable and Secure Computing, 2015, 12, 675-687.	3.7	35
9	A low-power ROM using charge recycling and charge sharing techniques. IEEE Journal of Solid-State Circuits, 2003, 38, 641-653.	3.5	33
10	An Energy-Efficient Deep Convolutional Neural Network Training Accelerator for In Situ Personalization on Smart Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2691-2702.	3.5	32
11	Multiple clone row DRAM. , 2015, , .		31
12	An SoC With 1.3 Gtexels/s 3-D Graphics Full Pipeline for Consumer Applications. IEEE Journal of Solid-State Circuits, 2006, 41, 71-84.	3.5	30
13	A 21-Gbit/s 1.63-pJ/bit Adaptive CTLE and One-Tap DFE With Single Loop Spectrum Balancing Method. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 789-793.	2.1	28
14	Energy-Efficient Design of Processing Element for Convolutional Neural Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1332-1336.	2.2	25
15	A Kernel Decomposition Architecture for Binary-weight Convolutional Neural Networks. , 2017, , .		25
16	NAND-Net: Minimizing Computational Complexity of In-Memory Processing for Binary Neural Networks. , 2019, , .		25
17	A high-resolution synchronous mirror delay using successive approximation register. IEEE Journal of Solid-State Circuits, 2004, 39, 1997-2004.	3.5	22
18	A 5-Gb/s/pin Transceiver for DDR Memory Interface With a Crosstalk Suppression Scheme. IEEE Journal of Solid-State Circuits, 2009, 44, 2222-2232.	3.5	20

#	Article	IF	Citations
19	Secure Encounter-Based Mobile Social Networks: Requirements, Designs, and Tradeoffs. IEEE Transactions on Dependable and Secure Computing, 2013, 10, 380-393.	3.7	20
20	A low-power charge-recycling ROM architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2003, 11, 590-600.	2.1	19
21	A 0.13-mum CMOS 6 Gb/s/pin Memory Transceiver Using Pseudo-Differential Signaling for Removing Common-Mode Noise Due to SSN. IEEE Journal of Solid-State Circuits, 2009, 44, 3146-3162.	3.5	19
22	A Data-Pattern-Tolerant Adaptive Equalizer Using the Spectrum Balancing Method. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 228-232.	2.2	19
23	A 5.4/2.7/1.62-Gb/s Receiver for DisplayPort Version 1.2 With Multi-Rate Operation Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2858-2866.	3.5	18
24	An Energy-Efficient Mobile Vertex Processor With Multithread Expanded VLIW Architecture and Vertex Caches. IEEE Journal of Solid-State Circuits, 2007, 42, 2257-2269.	3.5	17
25	Homogeneous Stream Processors With Embedded Special Function Units for High-Utilization Programmable Shaders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1691-1704.	2.1	17
26	A Unified Graphics and Vision Processor With a 0.89 /spl mu/W/fps Pose Estimation Engine for Augmented Reality. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 206-216.	2.1	17
27	An Optimized Design Technique of Low-bit Neural Network Training for Personalization on IoT Devices. , 2019, , .		17
28	A minimized hardware architecture of fast Phong shader using Taylor series approximation in 3D graphics. , 0, , .		16
29	A Spread Spectrum Clock Generator for DisplayPort Main Link. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 361-365.	2.2	16
30	A new crosstalk compensation method in line inversion TFT-LCD's. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1997, 44, 552-555.	0.1	14
31	A DLL With Jitter Reduction Techniques and Quadrature Phase Generation for DRAM Interfaces. IEEE Journal of Solid-State Circuits, 2009, 44, 1522-1530.	3.5	14
32	An Input Data and Power Noise Inducing Clock Jitter Tolerant Reference-Less Digital CDR for LCD Intra-Panel Interface. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 823-835.	3.5	14
33	A low-power ROM using single charge-sharing capacitor and hierarchical bit line. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 313-322.	2.1	13
34	A high resolution metastability-independent two-step gated ring oscillator TDC with enhanced noise shaping. , 2010, , .		13
35	MRTP: Mobile Ray Tracing Processor With Reconfigurable Stream Multi-Processors for High Datapath Utilization. IEEE Journal of Solid-State Circuits, 2012, 47, 518-535.	3.5	13
36	TrainWare. , 2018, , .		13

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37	A Reconfigurable SIMT Processor for Mobile Ray Tracing With Contention Reduction in Shared Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 938-950.	3.5	12
38	A real-time wavelet vector quantization algorithm and its VLSI architecture. IEEE Transactions on Circuits and Systems for Video Technology, 2000, 10, 475-489.	5.6	10
39	A 20 Gb/s 1:4 DEMUX Without Inductors and Low-Power Divide-by-2 Circuit in 0.13 $mu{hbox {m}}$ CMOS Technology. IEEE Journal of Solid-State Circuits, 2008, 43, 541-549.	3.5	10
40	A 116 fps/74 mW Heterogeneous 3D-Media Processor for 3-D Display Applications. IEEE Journal of Solid-State Circuits, 2010, 45, 652-667.	3.5	10
41	A 5-Gb/s Digital Clock and Data Recovery Circuit With Reduced DCO Supply Noise Sensitivity Utilizing Coupling Network. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 380-384.	2.1	10
42	A 0.9-V 12-Gb/s Two-FIR Tap Direct DFE With Feedback-Signal Common-Mode Control. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 724-728.	2.1	10
43	S-FLASH: A NAND Flash-based Deep Neural Network Accelerator Exploiting Bit-level Sparsity. IEEE Transactions on Computers, 2021, , 1-1.	2.4	10
44	A hardware cost minimized fast Phong shader. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001, 9, 297-304.	2.1	9
45	A 5.4-Gb/s Clock and Data Recovery Circuit Using Seamless Loop Transition Scheme With Minimal Phase Noise Degradation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2518-2528.	3.5	9
46	DRAM-Latency Optimization Inspired by Relationship between Row-Access Time and Refresh Timing. IEEE Transactions on Computers, 2016, 65, 3027-3040.	2.4	9
47	A Dual-Shader 3-D Graphics Processor With Fast 4-D Vector Inner Product Units and Power-Aware Texture Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 525-537.	2.1	8
48	An Adaptive Equalizer With the Capacitance Multiplication for DisplayPort Main Link in 0.18-mum CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 964-968.	2.1	8
49	Hybrid Temperature Sensor Network for Area-Efficient On-Chip Thermal Map Sensing. IEEE Journal of Solid-State Circuits, 2015, 50, 610-618.	3.5	8
50	An 11.5 Gb/s 1/4th Baud-Rate CTLE and Two-Tap DFE With Boosted High Frequency Gain in 110-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 588-592.	2.1	8
51	Adaptive selection of an index in a texture cache. , 0, , .		7
52	An integrated time register and arithmetic circuit with combined operation for time-domain signal processing. , 2015, , .		7
53	A 21%-Jitter-Improved Self-Aligned Dividerless Injection-Locked PLL With a VCO Control Voltage Ripple-Compensated Phase Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 733-737.	2.2	7
54	Q-DRAM: Quick-Access DRAM with Decoupled Restoring from Row-Activation. IEEE Transactions on Computers, 2016, 65, 2213-2227.	2.4	7

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55	A 36 fps SXGA 3-D Display Processor Embedding a Programmable 3-D Graphics Rendering Engine. IEEE Journal of Solid-State Circuits, 2008, 43, 1247-1259.	3.5	6
56	A Reconfigurable Heterogeneous Multimedia Processor for IC-Stacking on Si-Interposer. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 589-604.	5.6	6
57	PowerField: A Probabilistic Approach for Temperature-to-Power Conversion Based on Markov Random Field Theory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1509-1519.	1.9	6
58	A vision processor with a unified interest point detection and matching hardware for accelerating stereo matching algorithm. IEEE Transactions on Circuits and Systems for Video Technology, 2015, , 1-1.	5.6	6
59	DC-PCM: Mitigating PCM Write Disturbance with Low Performance Overhead by Using Detection Cells. IEEE Transactions on Computers, 2019, 68, 1741-1754.	2.4	6
60	Sparse-Insertion Write Cache to Mitigate Write Disturbance Errors in Phase Change Memory. IEEE Transactions on Computers, 2019, 68, 752-764.	2.4	6
61	CREMON: Cryptography Embedded on the Convolutional Neural Network Accelerator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3337-3341.	2.2	6
62	A Framework for Accelerating Transformer-Based Language Model on ReRAM-Based Architecture. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3026-3039.	1.9	6
63	An Area Efficient Early ${Z}$-Test Method for 3-D Graphics Rendering Hardware. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 1929-1938.	3.5	5
64	Computing energy-efficiency in the mobile GPU. , 2013, , .		5
65	A 6.5-Gb/s 1-mW/Gb/s/CH Simple Capacitive Crosstalk Compensator in a 130-nm Process. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 302-306.	2.2	5
66	A 10-Gb/s 0.71-pJ/bit Forwarded-Clock Receiver Tolerant to High-Frequency Jitter in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 264-268.	2.2	5
67	A PVT-robust Customized 4T Embedded DRAM Cell Array for Accelerating Binary Neural Networks. , 2019, , .		5
68	Amnesiac DRAM: A Proactive Defense Mechanism Against Cold Boot Attacks. IEEE Transactions on Computers, 2021, 70, 539-551.	2.4	5
69	Fault-free: A Fault-resilient Deep Neural Network Accelerator based on Realistic ReRAM Devices. , 2021, , .		5
70	A Pragmatic Approach to On-device Incremental Learning System with Selective Weight Updates. , 2020, , .		5
71	Comments on "New dynamic flip-flops for high-speed dual-modulus prescaler". IEEE Journal of Solid-State Circuits, 2000, 35, 919-920.	3.5	4
72	A cost-effective VLSI architecture for anisotropic texture filtering in limited memory bandwidth. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 254-267.	2.1	4

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73	An area efficient asynchronous gated ring oscillator TDC with minimum GRO stages. , 2010, , .		4
74	A 20 Gbps 1-tap decision feedback equalizer with unfixed tap coefficient. , 2012, , .		4
75	Peer Pressure: Exerting Malicious Influence on Routers at a Distance. , 2013, , .		4
76	A Quarter-Rate Forwarded Clock Receiver Based on ILO With Low Jitter Tracking Bandwidth Variation Using Phase Shifting Phenomenon in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2482-2490.	3.5	4
77	A 9.6-Gb/s 1.22-mW/Gb/s Data-Jitter Mixing Forwarded-Clock Receiver in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2023-2033.	2.1	4
78	A 9.6 Gb/s 0.96 mW/Gb/s Forwarded Clock Receiver With High Jitter Tolerance Using Mixing Cell Integrated Injection-Locked Oscillator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2495-2503.	3.5	4
79	Elaborate Refresh: A Fine Granularity Retention Management for Deep Submicron DRAMs. IEEE Transactions on Computers, 2018, 67, 1403-1415.	2.4	4
80	A 0.65-V, 11.2-Gb/s Power Noise Tolerant Source-Synchronous Injection-Locked Receiver With Direct DTLB DFE. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1564-1568.	2.2	4
81	eSRCNN: A Framework for Optimizing Super-Resolution Tasks on Diverse Embedded CNN Accelerators. , 2019, , .		4
82	An Energy-efficient Processing-in-memory Architecture for Long Short Term Memory in Spin Orbit Torque MRAM. , 2019, , .		4
83	A Deep Neural Network Training Architecture With Inference-Aware Heterogeneous Data-Type. IEEE Transactions on Computers, 2022, 71, 1216-1229.	2.4	4
84	Semi-recursive VLSI architecture for two dimensional discrete wavelet transform. , 0, , .		3
85	Area-efficient dynamic thermal management unit using MDLL with shared DLL scheme for many-core processors. , 2011, , .		3
86	A 5.4 Gb/s clock and data recovery circuit using the seamless loop transition scheme without phase noise degradation. , 2011, , .		3
87	A 5 Gbps 1.6 mW/G bps/CH Adaptive Crosstalk Cancellation Scheme With Reference-less Digital Calibration and Switched Termination Resistors for Single-Ended Parallel Interface. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3016-3024.	3.5	3
88	Private Over-Threshold Aggregation Protocols over Distributed Datasets. IEEE Transactions on Knowledge and Data Engineering, 2016, 28, 2467-2479.	4.0	3
89	SENIN: An energy-efficient sparse neuromorphic system with on-chip learning. , 2017, , .		3
90	Low power pipelined FFT architecture for synthetic aperture radar signal processing. , 0, , .		2

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91	An area-efficient on-chip temperature sensor with nonlinearity compensation using injection-locked oscillator (ILO). , 2014, , .		2
92	Hijacking the Vuze BitTorrent network: all your hop are belong to us. IET Information Security, 2015, 9, 203-208.	1.1	2
93	Refresh-Aware Write Recovery Memory Controller. IEEE Transactions on Computers, 2017, 66, 688-701.	2.4	2
94	In-DRAM Data Initialization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3251-3254.	2.1	2
95	A 12 Gb/s 1.59 mW/Gb/s Input-Data-Jitter-Tolerant Injection-Type CDR With Super-Harmonic Injection-Locking in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1972-1976.	2.2	2
96	A 47.4ÂµJ/epoch Trainable Deep Convolutional Neural Network Accelerator for In-Situ Personalization on Smart Devices. , 2019, , .		2
97	A 10.8 Gb/s Quarter-Rate 1 FIR 1 IIR Direct DFE With Non-Time-Overlapping Data Generation for 4:1 CMOS Clockless Multiplexer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 67-71.	2.2	2
98	A Framework for Area-efficient Multi-task BERT Execution on ReRAM-based Accelerators. , 2021, , .		2
99	A mode-changeable 2-D DCT/IDCT processor for digital VCR. IEEE Transactions on Consumer Electronics, 1996, 42, 606-616.	3.0	1
100	Buck converter with a new driving circuit in a TV power system. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1996, 43, 811-813.	0.1	1
101	High speed, energy efficient master-slave flip-flops. , 0, , .		1
102	A Mobile 3-D Display Processor With A Bandwidth-Saving Subdivider. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1082-1093.	2.1	1
103	A 7 mW 2.5 GHz spread spectrum clock generator using switch-controlled injection-locked oscillator. , 2013, , .		1
104	A LOG-Induced SSN-Tolerant Transceiver for On-Chip Interconnects in COG-Packaged Source Driver IC for TFT-LCD. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 21-25.	2.2	1
105	A Forwarded-Clock Receiver With Constant and Wide-Range Jitter-Tracking Bandwidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 153-157.	2.2	1
106	Bank-Group Level Parallelism. IEEE Transactions on Computers, 2017, 66, 1428-1434.	2.4	1
107	A 10-Gb/s Reference-Less Baud-Rate CDR for Low Power Consumption With the Direct Feedback Method. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1539-1543.	2.2	1
108	Compressing Sparse Ternary Weight Convolutional Neural Networks for Efficient Hardware Acceleration. , 2019, , .		1

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109	Quantization-Error-Robust Deep Neural Network for Embedded Accelerators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 609-613.	2.2	1
110	Deferred Dropout: An Algorithm-Hardware Co-Design DNN Training Method Provisioning Consistent High Activation Sparsity. , 2021, , .		1
111	Energy-Efficient CNN Personalized Training by Adaptive Data Reformation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 332-336.	1.9	1
112	An ASIC implementation of range cell migration compensation algorithm for synthetic aperture radar signal processing. , 0, , .		0
113	A new 4-2 adder and booth selector for low power MAC unit. , 0, , .		0
114	VLSI implementation of decoder for decompressing fractal-based compressed image. , 0, , .		0
115	VLSI implementation of Phong shader in 3D graphics. , 0, , .		0
116	Self-timed shared division and square-root implementation using full redundant signed digit numbers. , 0, , .		0
117	Application specific embedded 8-Port SRAM with simultaneous 256-bit data accessibility. , 0, , .		0
118	A 1mJ/frame unified media application processor with a 179.7pJ mixed-mode feature extraction engine for embedded 3D-media contents processing. , 2012, , .		0
119	Timing error masking by exploiting operand value locality in SIMD architecture. , 2014, , .		0
120	A Forwarded Clock Receiver Based on Injection-Locked Oscillator With AC-Coupled Clock Multiplication Unit in <inline-formula> <tex-math notation="LaTeX">$0.13~oldsymbol {mu } $ </tex-math></inline-formula>m CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 988-992.	2.1	0
121	Crosstalk avoidance code for direct pass-through architecture. , 2016, , .		0
122	Rare Computing: Removing Redundant Multiplications From Sparse and Repetitive Data in Deep Neural Networks. IEEE Transactions on Computers, 2022, 71, 795-808.	2.4	0
123	Enabling the Large-Scale Emulation of Internet of Things Firmware With Heuristic Workarounds. IEEE Security and Privacy, 2021, , 2-11.	1.5	0