

Pingqiang Zhou

List of Publications by Year in descending order

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Version: 2024-02-01

36
papers

155
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times ranked

105
citing authors

| # | ARTICLE | IF | CITATIONS |
|----|---|-----|-----------|
| 1 | Thermal-Aware Layout Optimization and Mapping Methods for Resistive Neuromorphic Engines. , 2022, , . | | 2 |
| 2 | A Quantized Training Framework for Robust and Accurate ReRAM-based Neural Network Accelerators. , 2021, , . | | 5 |
| 3 | Efficient Techniques for Training the Memristor-based Spiking Neural Networks Targeting Better Speed, Energy and Lifetime. , 2021, , . | | 2 |
| 4 | The Study of TSV-Induced and Strained Silicon-Enhanced Stress in 3D-IC. , 2021, , . | | 0 |
| 5 | Parasitic Capacitance Modeling of Si-Bulk FinFET-Based pMOS. IEEE Transactions on Electron Devices, 2021, 68, 4819-4825. | 1.6 | 5 |
| 6 | Efficient Techniques for Extending Service Time for Memristor-based Neural Networks. , 2021, , . | | 1 |
| 7 | Detecting Adversarial Examples Utilizing Pixel Value Diversity. , 2021, , . | | 2 |
| 8 | Early-Stage Planning of Switched-Capacitor Converters in a Heterogeneous Chip. IEEE Access, 2020, 8, 85900-85911. | 2.6 | 1 |
| 9 | Defending Against Adversarial Attacks in Deep Learning with Robust Auxiliary Classifiers Utilizing Bit Plane Slicing. , 2020, , . | | 0 |
| 10 | Improved Hierarchical IR Drop Analysis in Homogeneous Circuits. , 2020, , . | | 2 |
| 11 | An Improved Design of Hybrid Integrated Voltage Regulator Based on DLDO and SCVR. , 2020, , . | | 0 |
| 12 | Effective Activating Compensation Logic for Drams in 3D-ICs. , 2019, , . | | 1 |
| 13 | A Cross-Layer Framework for Temporal Power and Supply Noise Prediction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1914-1927. | 1.9 | 2 |
| 14 | Customized High Performance and Energy Efficient Communication Networks for AI Chips. IEEE Access, 2019, 7, 69434-69446. | 2.6 | 10 |
| 15 | Optimizing the Energy Efficiency of Power Supply in Heterogeneous Multicore Chips with Integrated Switched-Capacitor Converters. , 2019, , . | | 4 |
| 16 | A Compact Memory Structure based on 2T1R Against Single-Event Upset in RRAM Arrays. , 2019, , . | | 1 |
| 17 | CoDRAM: A Novel Near Memory Computing Framework with Computational DRAM. , 2019, , . | | 1 |
| 18 | Addressing Aging Issues in Heterogeneous Three-Dimensional Integrated Circuits. , 2019, , . | | 0 |

| # | ARTICLE | IF | CITATIONS |
|----|--|-----|-----------|
| 19 | Deep Learning for Spatial Supply Noise Estimation in a Processor Chip. , 2018, , . | | 1 |
| 20 | An improved leakage-driven runtime decap modulation algorithm for microprocessors. , 2018, , . | | 0 |
| 21 | Integrating low-resolution surveillance camera and smartphone inertial sensors for indoor positioning. , 2018, , . | | 3 |
| 22 | An outlier detection method and its application to multicore-chip power estimation. , 2017, , . | | 1 |
| 23 | How secure is split manufacturing in preventing hardware trojan?. , 2016, , . | | 3 |
| 24 | Machine Learning for Noise Sensor Placement and Full-Chip Voltage Emergency Detection. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1. | 1.9 | 5 |
| 25 | Design and cad of noise sensors for on-die supply voltage emergency detection. , 2016, , . | | 1 |
| 26 | Leakage power reduction in multicore chips via online decap modulation. , 2016, , . | | 3 |
| 27 | A statistical methodology for noise sensor placement and full-chip voltage map generation. , 2015, , . | | 7 |
| 28 | Design and optimization of on-chip voltage regulators for high performance applications. , 2014, , . | | 1 |
| 29 | Distributed On-Chip Switched-Capacitor DC-DC Converters Supporting DVFS in Multicore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1954-1967. | 2.1 | 19 |
| 30 | Placement Optimization of Power Supply Pads Based on Locality. , 2013, , . | | 1 |
| 31 | Optimization of on-chip switched-capacitor DC-DC converters for high-performance applications. , 2012, , . | | 11 |
| 32 | NoC frequency scaling with flexible-pipeline routers. , 2011, , . | | 10 |
| 33 | Exploration of on-chip switched-capacitor DC-DC converter for multicore processors using a distributed power delivery network. , 2011, , . | | 16 |
| 34 | THERMAL IMPACTS OF LEAKAGE POWER IN 2D/3D FLOORPLANNING. Journal of Circuits, Systems and Computers, 2010, 19, 1483-1495. | 1.0 | 0 |
| 35 | Application-specific 3D Network-on-Chip design using simulated allocation. , 2010, , . | | 4 |
| 36 | Congestion-aware power grid optimization for 3D circuits using MIM and CMOS decoupling capacitors. , 2009, , . | | 30 |