

Chi On Chui

List of Publications by Year in descending order

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100
papers

4,126
citations

159525

30
h-index

123376

61
g-index

101
all docs

101
docs citations

101
times ranked

3482
citing authors

#	ARTICLE	IF	CITATIONS
1	Nanoparticles suppress fluid instabilities in the thermal drawing of ultralong nanowires. Nature Communications, 2020, 11, 5932.	5.8	2
2	Wideband Frequency Reconfigurable Patch Antenna With Switchable Slots Based on Liquid Metal and 3-D Printed Microfluidics. IEEE Transactions on Antennas and Propagation, 2019, 67, 2886-2895.	3.1	78
3	Engineering finger-operated peristaltic pumps. Microfluidics and Nanofluidics, 2018, 22, 1.	1.0	5
4	Robust Density Matrix Simulation of Terahertz Quantum Cascade Lasers. IEEE Transactions on Terahertz Science and Technology, 2018, 8, 492-501.	2.0	10
5	Tunneling Negative Differential Resistance-Assisted STT-RAM for Efficient Read and Write Operations. IEEE Transactions on Electron Devices, 2017, 64, 121-129.	1.6	15
6	Density matrix modeling of quantum cascade lasers without an artificially localized basis: A generalized scattering approach. Physical Review B, 2017, 96, .	1.1	21
7	Leveraging nMOS Negative Differential Resistance for Low Power, High Reliability Magnetic Memory. IEEE Transactions on Electron Devices, 2017, 64, 4084-4090.	1.6	6
8	Self-Locking Optoelectronic Tweezers for Single-Cell and Microparticle Manipulation across a Large Area in High Conductivity Media. Scientific Reports, 2016, 6, 22630.	1.6	29
9	An Evaluation Framework for Nanotransfer Printing-Based Feature-Level Heterogeneous Integration in VLSI Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1858-1870.	2.1	2
10	Semiconductor Electronic Label-Free Assay for Predictive Toxicology. Scientific Reports, 2016, 6, 24982.	1.6	15
11	Carbon-ionogel supercapacitors for integrated microelectronics. Nanotechnology, 2016, 27, 035204.	1.3	3
12	PROCEED: A Pareto Optimization-Based Circuit-Level Evaluator for Emerging Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 192-205.	2.1	7
13	Gate-Induced Source Tunneling FET (GISTFET). IEEE Transactions on Electron Devices, 2015, 62, 2390-2395.	1.6	4
14	Junctionless Silicon and In _{0.53} Ga _{0.47} As Transistorsâ€™ Part II: Device Variability From Random Dopant Fluctuation. IEEE Transactions on Electron Devices, 2015, 62, 3208-3214.	1.6	15
15	Modeling source-drain tunneling in ultimately scaled IIIâ€™V transistors. Applied Physics Letters, 2015, 106, .	1.5	5
16	Scaled carbon-ionogel supercapacitors for electronic circuits. , 2014, , .		1
17	Understanding and optimization of the sensitivity of nanoscale FET-based biosensors. , 2014, , .		1
18	PROCEED: A pareto optimization-based circuit-level evaluator for emerging devices. , 2014, , .		6

#	ARTICLE	IF	CITATIONS
19	RF performance limits of ballistic Si field-effect transistors. , 2014, , .		1
20	Modeling direct interband tunneling. II. Lower-dimensional structures. Journal of Applied Physics, 2014, 116, .	1.1	25
21	On the origin of enhanced sensitivity in nanoscale FET-based biosensors. Proceedings of the National Academy of Sciences of the United States of America, 2014, 111, 5111-5116.	3.3	161
22	Modeling direct interband tunneling. I. Bulk semiconductors. Journal of Applied Physics, 2014, 116, .	1.1	15
23	Evaluation of Digital Circuit-Level Variability in Inversion-Mode and Junctionless FinFET Technologies. IEEE Transactions on Electron Devices, 2013, 60, 2186-2193.	1.6	27
24	A systematic approach for hydrodynamic model calibration in the quasi-ballistic regime. Solid-State Electronics, 2013, 87, 90-97.	0.8	1
25	Interactions Between Line Edge Roughness and Random Dopant Fluctuation in Nonplanar Field-Effect Transistor Variability. IEEE Transactions on Electron Devices, 2013, 60, 3277-3284.	1.6	35
26	Stochastic Variability in Silicon Double-Gate Lateral Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2013, 60, 84-91.	1.6	66
27	Electrostatic Modeling and Insights Regarding Multigate Lateral Tunneling Transistors. IEEE Transactions on Electron Devices, 2013, 60, 2712-2720.	1.6	43
28	Ultrasensitive biomolecular assays with amplifying nanowire FET biosensors. , 2013, , .		0
29	Nanowire field-programmable computing platform. , 2013, , .		0
30	CMOS Junctionless Field-Effect Transistors Manufacturing Cost Evaluation. IEEE Transactions on Semiconductor Manufacturing, 2013, 26, 162-168.	1.4	16
31	Analog/RF Performance and Optimization of Vertical III-V Double-Gate Transistor. IEEE Transactions on Electron Devices, 2013, 60, 1613-1618.	1.6	0
32	Variability in Nanoscale Fabrics. ACM Journal on Emerging Technologies in Computing Systems, 2013, 9, 1-24.	1.8	3
33	Variability in Nanoscale FinFET Technologies. Lecture Notes in Nanoscale Science and Technology, 2013, , 159-203.	0.4	2
34	Heterogeneous integration of epitaxial nanostructures: strategies and application drivers. , 2012, , .		3
35	Channel length dependent sensitivity of Schottky contacted silicon nanowire field-effect transistor sensors. Applied Physics Letters, 2012, 100, 123504.	1.5	10
36	On-chip variation sensor for systematic variation estimation in nanoscale fabrics. , 2012, , .		1

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37	Variability Impact of Random Dopant Fluctuation on Nanoscale Junctionless FinFETs. IEEE Electron Device Letters, 2012, 33, 767-769.	2.2	157
38	Integrated Deviceâ€“Fabric Explorations and Noise Mitigation in Nanoscale Fabrics. IEEE Nanotechnology Magazine, 2012, 11, 687-700.	1.1	14
39	Phase-Change Memory With Multifin Thin-Film-Transistor Driver Technology. IEEE Electron Device Letters, 2012, 33, 405-407.	2.2	4
40	A Quasi-Analytical Model for Double-Gate Tunneling Field-Effect Transistors. IEEE Electron Device Letters, 2012, 33, 1468-1470.	2.2	66
41	Optimization of the Sensitivity of FET-Based Biosensors via Biasing and Surface Charge Engineering. IEEE Transactions on Electron Devices, 2012, 59, 3104-3110.	1.6	48
42	Transient measurement approaches to differentiate non-specific binding in affinity-based bioanalytical assays. Journal of Applied Physics, 2012, 112, 024702.	1.1	0
43	Nanomanufacturing Strategy for Aligned Assembly of Nanowire Arrays. Journal of Electronic Materials, 2012, 41, 935-943.	1.0	1
44	One-Time-Programmable Memory in LTPS TFT Technology With Metal-Induced Lateral Crystallization. IEEE Transactions on Electron Devices, 2012, 59, 145-150.	1.6	3
45	Device- and Circuit-Level Variability Caused by Line Edge Roughness for Sub-32-nm FinFET Technologies. IEEE Transactions on Electron Devices, 2012, 59, 2057-2063.	1.6	44
46	Variability of Inversion-Mode and Junctionless FinFETs due to Line Edge Roughness. IEEE Electron Device Letters, 2011, 32, 1489-1491.	2.2	71
47	Nanoscale Application Specific Integrated Circuits. , 2011, , .		12
48	Integrated nanosystems with junctionless crossed nanowire transistors. , 2011, , .		5
49	A stacked memory device on logic 3D technology for ultra-high-density data storage. Nanotechnology, 2011, 22, 254006.	1.3	48
50	Integrated amplifying nanowire FET for surface and bulk sensing. , 2011, , .		0
51	3D integrable nanowire FET sensor with intrinsic sensitivity boost. , 2011, , .		4
52	Nanoscale Application-Specific Integrated Circuits. , 2011, , 215-275.		16
53	Mechanism for excess noise in mixed tunneling and avalanche breakdown of silicon. Applied Physics Letters, 2010, 96, 263503.	1.5	2
54	Parameter Variability in Nanoscale Fabrics: Bottom-Up Integrated Exploration. , 2010, , .		8

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55	High Mobility Compound Semiconductor Permeable Base Transistors with Suppressed Base Current. ECS Transactions, 2010, 33, 93-101.	0.3	1
56	Schottky Contacted Nanowire Field-Effect Sensing Device With Intrinsic Amplification. IEEE Electron Device Letters, 2010, , .	2.2	7
57	Insights and optimizations of tunnel field-effect transistor operation. , 2009, , .		3
58	Validating cascading of crossbar circuits with an integrated device-circuit exploration. , 2009, , .		17
59	Novel T-channel nanowire FET with built-in signal amplification for pH sensing. , 2009, , .		5
60	On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates. IEEE Transactions on Electron Devices, 2008, 55, 547-556.	1.6	339
61	The low subthreshold swing possibility with asymmetries in double-gate SOI MOSFET. , 2008, , .		0
62	Low dissipation nanoscale transistor physics and operations. , 2008, , .		0
63	Nanoscale Germanium MOS Dielectrics and Junctions. , 2007, , 295-361.		3
64	Advanced Germanium MOS Devices. , 2007, , 363-386.		4
65	Interface Layers for High-k/Ge Gate Stacks: Are They Necessary?. ECS Meeting Abstracts, 2006, , .	0.0	0
66	High performance germanium MOSFETs. Materials Science and Engineering B: Solid-State Materials for Advanced Technology, 2006, 135, 242-249.	1.7	126
67	Nanoscale germanium MOS Dielectrics-part I: germanium oxynitrides. IEEE Transactions on Electron Devices, 2006, 53, 1501-1508.	1.6	120
68	Nanoscale germanium MOS Dielectrics-part II: high- κ gate dielectrics. IEEE Transactions on Electron Devices, 2006, 53, 1509-1516.	1.6	90
69	High Mobility Materials and Novel Device Structures for High Performance Nanoscale MOSFETs. , 2006, , .		65
70	Leakage suppression by asymmetric area electrodes in metal-semiconductor-metal photodetectors. Applied Physics Letters, 2006, 88, 063506.	1.5	20
71	PERFORMANCE LIMITATIONS OF Si CMOS AND ALTERNATIVES FOR NANOELECTRONICS. International Journal of High Speed Electronics and Systems, 2006, 16, 175-192.	0.3	2
72	PERFORMANCE LIMITATIONS OF Si CMOS AND ALTERNATIVES FOR NANOELECTRONICS. , 2006, , .		0

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73	A novel technique to reduce leakage in metal-semiconductor metal photodetectors. , 2005, , .		0
74	Ge based high performance nanoscale MOSFETs. Microelectronic Engineering, 2005, 80, 15-21.	1.1	118
75	Germanium n-type shallow junction activation dependences. Applied Physics Letters, 2005, 87, 091909.	1.5	169
76	Characteristics and mechanism of tunable work function gate electrodes using a bilayer metal structure on SiO ₂ / and HfO ₂ /sub 2/. IEEE Electron Device Letters, 2005, 26, 445-447.	2.2	62
77	High mobility Ge pMOS fabricated using a novel heteroepitaxial ge on Si growth method. , 2005, , .		0
78	Zirconia-germanium interface photoemission spectroscopy using synchrotron radiation. Journal of Applied Physics, 2005, 97, 113518.	1.1	34
79	Fabrication of high-quality p-MOSFET in Ge grown heteroepitaxially on Si. IEEE Electron Device Letters, 2005, 26, 311-313.	2.2	83
80	Interfacial characteristics of HfO ₂ grown on nitrided Ge (100) substrates by atomic-layer deposition. Applied Physics Letters, 2004, 85, 2902-2904.	1.5	131
81	Zirconia grown by ultraviolet ozone oxidation on germanium (100) substrates. Journal of Applied Physics, 2004, 96, 813-819.	1.1	40
82	Integration of Optical Polymer Pillars Chip I/O Interconnections with Si MSM Photodetectors. IEEE Transactions on Electron Devices, 2004, 51, 1084-1090.	1.6	9
83	Scalability and Electrical Properties of Germanium Oxynitride MOS Dielectrics. IEEE Electron Device Letters, 2004, 25, 613-615.	2.2	102
84	Engineering chemically abrupt high-k metal oxide-silicon interfaces using an oxygen-gettering metal overlayer. Journal of Applied Physics, 2004, 96, 3467-3472.	1.1	182
85	Atomic Layer Deposition of High- κ Dielectric for Germanium MOS Applications-Substrate Surface Preparation. IEEE Electron Device Letters, 2004, 25, 274-276.	2.2	120
86	Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality. Applied Physics Letters, 2004, 85, 2815-2817.	1.5	146
87	Effective dark current suppression with asymmetric MSM photodetectors in Group IV semiconductors. IEEE Photonics Technology Letters, 2003, 15, 1585-1587.	1.3	111
88	Activation and diffusion studies of ion-implanted p and n dopants in germanium. Applied Physics Letters, 2003, 83, 3275-3277.	1.5	275
89	Local epitaxial growth of ZrO ₂ on Ge (100) substrates by atomic layer epitaxy. Applied Physics Letters, 2003, 83, 2647-2649.	1.5	126
90	Germanium MOS capacitors incorporating ultrathin high- κ gate dielectric. IEEE Electron Device Letters, 2002, 23, 473-475.	2.2	316

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91	Thermal analysis of heterogeneous 3D ICs with various integration scenarios. , 0, , .		29
92	A sub-400Å°C germanium MOSFET technology with high- ϵ dielectric and metal gate. , 0, , .		65
93	Ultrathin high- ϵ gate dielectric technology for germanium MOS applications. , 0, , .		4
94	A germanium NMOSFET process integrating metal gate and improved hi- ϵ dielectrics. , 0, , .		18
95	A novel self-aligned gate-last MOSFET process comparing high-K candidates. , 0, , .		1
96	Electro-thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs. , 0, , .		25
97	Advanced germanium MOSFET technologies with high- ϵ gate dielectrics and shallow junctions. , 0, , .		3
98	Advanced Germanium MOS Devices and Technology. , 0, , .		1
99	Dual stress capping layer enhancement study for hybrid orientation finFET CMOS technology. , 0, , .		13
100	Synthesized compact model and experimental results for substrate noise coupling in lightly doped processes. , 0, , .		4