Padmanabhan Balasubramanian

List of Publications by Year
in descending order

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77	447	933264	996849
papers	citations	10 h-index	15 g-index

82	82	82	149
all docs	docs citations	times ranked	citing authors

#	ARTICLE	IF	CITATIONS
1	Hardware Optimized and Error Reduced Approximate Adder. Electronics (Switzerland), 2019, 8, 1212.	1.8	26
2	Low power digital design using modified GDI method. , 2006, , .		23
3	A distributed minority and majority voting based redundancy scheme. Microelectronics Reliability, 2015, 55, 1373-1378.	0.9	23
4	Performance Comparison of Carry-Lookahead and Carry-Select Adders Based on Accurate and Approximate Additions. Electronics (Switzerland), 2018, 7, 369.	1.8	23
5	An Approximate Adder With a Near-Normal Error Distribution: Design, Error Analysis and Practical Application. IEEE Access, 2021, 9, 4518-4530.	2.6	20
6	A delay efficient robust self-timed full adder. , 2008, , .		19
7	A latency optimized biased implementation style weak-indication self-timed full adder. Facta Universitatis - Series Electronics and Energetics, 2015, 28, 657-671.	0.6	19
8	Approximate ripple carry and carry lookahead adders â€" A comparative analysis. , 2017, , .		15
9	SELF-TIMED SECTION-CARRY BASED CARRY LOOKAHEAD ADDERS AND THE CONCEPT OF ALIAS LOGIC. Journal of Circuits, Systems and Computers, 2013, 22, 1350028.	1.0	13
10	Comments on â€œDual-rail asynchronous logic multi-level implementationâ€• The Integration VLSI Journal, 2016, 52, 34-40.	1.3	13
11	Hardware Efficient Approximate Adder Design. , 2018, , .		11
12	Low Power Robust Early Output Asynchronous Block Carry Lookahead Adder with Redundant Carry Logic. Electronics (Switzerland), 2018, 7, 243.	1.8	11
13	Hardware Optimized Approximate Adder with Normal Error Distribution. , 2020, , .		11
14	Approximate Array Multipliers. Electronics (Switzerland), 2021, 10, 630.	1.8	11
15	Comparative evaluation of quasi-delay-insensitive asynchronous adders corresponding to return-to-zero and return-to-one handshaking. Facta Universitatis - Series Electronics and Energetics, 2018, 31, 25-39.	0.6	11
16	Area/latency optimized early output asynchronous full adders and relative-timed ripple carry adders. SpringerPlus, 2016, 5, 440.	1.2	10
17	Generalized Majority Voter Design Method for N-Modular Redundant Systems Used in Mission- and Safety-Critical Applications. Computers, 2019, 8, 10.	2.1	10
18	Efficient Realization of Strongly Indicating Function Blocks. , 2008, , .		9

#	Article	IF	Citations
19	A New Design Technique for Weakly Indicating Function Blocks. , 2008, , .		9
20	Power, delay and area efficient self-timed multiplexer and demultiplexer designs. , 2009, , .		8
21	Redundant Logic Insertion and Latency Reduction in Self-Timed Adders. VLSI Design, 2012, 2012, 1-13.	0.5	8
22	Asynchronous carry select adders. Engineering Science and Technology, an International Journal, 2017, 20, 1066-1074.	2.0	8
23	Redundant logic insertion and fault tolerance improvement in combinational circuits. , 2017, , .		8
24	FPGA-Based Synthesis of High-Speed Hybrid Carry Select Adders. Advances in Electronics, 2015, 2015, 1-13.	1.9	7
25	Speed, energy and area optimized early output quasi-delay-insensitive array multipliers. PLoS ONE, 2020, 15, e0228343.	1.1	7
26	Design of combinational logic digital circuits using a mixed logic synthesis method. , 0, , .		6
27	FPGA implementation of synchronous section-carry based carry look-ahead adders. , 2014, , .		6
28	Majority and Minority Voted Redundancy Scheme for Safety-Critical Applications with Error/No-Error Signaling Logic. Electronics (Switzerland), 2018, 7, 272.	1.8	6
29	Early Output Quasi-Delay-Insensitive Array Multipliers. Electronics (Switzerland), 2019, 8, 444.	1.8	6
30	Building a System for Arabic Dialects Identification based on Speech Recognition using Hidden Markov Models (HMMs). , 2021, 1, 53-65.		6
31	Low power self-timed carry lookahead adders. , 2013, , .		5
32	ASIC-based design of NMR system health monitor for mission/safetyâ€“critical applications. SpringerPlus, 2016, 5, 628.	1.2	5
33	Majority and Minority Voted Redundancy for Safety-Critical Applications. , 2018, , .		5
34	A Self-Healing Redundancy Scheme for Mission/Safety-Critical Applications. IEEE Access, 2018, 6, 69640-69649.	2.6	5
35	Factorized Carry Lookahead Adders. , 2019, , .		5
36	Low Power Synthesis of XOR-XNOR Intensive Combinational Logic. , 2007, , .		4

#	Article	IF	Citations
37	A comparison of quasi-delay-insensitive asynchronous adder designs corresponding to return-to-zero and return-to-one handshaking. , 2017, , .		4
38	Asynchronous early output section-carry based carry lookahead adder with alias carry logic. , 2017, , .		4
39	Indicating Asynchronous Multipliers. , 2018, , .		4
40	Quasi Delay Insensitive Majority Voters for Triple Modular Redundancy Applications. Applied Sciences (Switzerland), 2019, 9, 5400.	1.3	4
41	Dual-Sum Single-Carry Self-Timed Adder Designs. , 2009, , .		3
42	Computation of Error Resiliency of Muller C-element. , 2014, , .		3
43	Speed and energy optimized quasi-delay-insensitive block carry lookahead adder. PLoS ONE, 2019, 14, e0218347.	1.1	3
44	Approximate Adder with Reduced Error. , 2019, , .		3
45	Analysis of non-adjacency in K-maps and its impact on power consumption reduction in non-regenerative CMOS circuits. , 2005, , .		2
46	Power optimized logic circuit design with a novel synthesis technique. , 0, , .		2
47	Self-timed full adder designs based on hybrid input encoding. , 2009, , .		2
48	On the Error Resiliency of Combinational Logic Cells - Implications for Nano-based Digital Design. , 2013, , .		2
49	Approximate quasi-delay-insensitive asynchronous adders: Design and analysis. , 2017, , .		2
50	Asynchronous early output majority voter and a relative-timed asynchronous TMR implementation. Microelectronics Reliability, 2020, 114, 113781.	0.9	2
51	Asynchronous quasi delay insensitive majority voters corresponding to quintuple modular redundancy for mission/safety-critical applications. PLoS ONE, 2020, 15, e0239395.	1.1	2
52	An Approximate Adder with Reduced Error and Optimized Design Metrics. , 2021, , .		2
53	Digital Image Compression Using Approximate Addition. Electronics (Switzerland), 2022, 11, 1361.	1.8	2
54	Heterogeneously encoded dual-bit self-timed adder. , 2009, , .		1

#	Article	IF	Citations
55	Dynamic CMOS Incrementers-cum-Decrementers Based on Least Significant Zero Bit Principle. , 2014, , .		1
56	A System Health Indicator for the Distributed Minority and Majority Voting Based Redundancy Scheme. , 2018, , .		1
57	Area Optimized Quasi Delay Insensitive Majority Voter for TMR Applications. , 2019, , .		1
58	Quasi-Delay-Insensitive Implementation of Approximate Addition. Symmetry, 2020, 12, 1919.	1.1	1
59	Gate-Level Static Approximate Adders: A Comparative Analysis. Electronics (Switzerland), 2021, 10, 2917.	1.8	1
60	Quasi delay insensitive implementation of approximate multiplication. Ain Shams Engineering Journal, 2022, 13, 101629.	3.5	1
61	Approximator: A Software Tool for Automatic Generation of Approximate Arithmetic Circuits. Computers, 2022, 11, 11.	2.1	1
62	Simultaneous delay optimization and depth reduction in logic trees with minimum resources. , 2006, , .		0
63	Simultaneous Delay optimization and Depth reduction in Logic trees with minimum resources. Midwest Symposium on Circuits and Systems, 2006, , .	1.0	0
64	EDP optimized synthesis scheme for Boolean read-once functions. , 2006, , .		0
65	Power aware minimization of complementary logic functions based on maximal HD. , 2006, , .		0
66	Synthesis of Power and Delay Optimized NIG structures. , 2007, , .		0
67	Totally self-checking checker modules revisited. , 2010, , .		0
68	Mathematical estimation of logical masking capability of majority/minority gates used in nanoelectronic circuits. , 2017, , .		0
69	Asynchronous Early Output Block Carry Lookahead Adder with Improved Quality of Results. , 2018, , .		0
70	Area, Power and Speed Optimized Early Output Majority Voter for Asynchronous TMR Implementation. Electronics (Switzerland), 2021, 10, 1425.	1.8	0
71	A Boolean Heuristic for Disjoint SOP Synthesis. , 2021, , .		0
72	Image Blending using Approximate Multiplication. , 2021, , .		0

#	Article	IF	Citations
73	On Deducing the Clique Potential of Nanoscale Combinational Circuits. Current Nanoscience, 2013, 9, 514-520.	0.7	0
74	Pollen Classification of Three Types of Plants of the Family Malvaceae Using Computational Intelligence Approach. , 2021, 1, 1-7.		0
75	Global versus Local Weak-Indication Self-Timed Function Blocks â€“ A Comparative Analysis. , 2021, 1, 17-28.		0
76	Design of 8-bit Dynamic CMOS Priority Resolvers based on Active- High and Active-Low Logic. WSEAS Transactions on Information Science and Applications, 2021, 18, 141-145.	0.2	0
77	Image Compression using Approximate Addition. , 2021, , .		0