

Fahim Rahman

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/2101840/publications.pdf>

Version: 2024-02-01

20
papers

307
citations

1478505

6
h-index

1588992

8
g-index

20
all docs

20
docs citations

20
times ranked

303
citing authors

#	ARTICLE	IF	CITATIONS
1	Introduction to Cyber-Physical System Security: A Cross-Layer Perspective. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 215-227.	2.4	66
2	An Aging-Resistant RO-PUF for Reliable Key Generation. IEEE Transactions on Emerging Topics in Computing, 2015, , 1-1.	4.6	64
3	SoC Security Verification using Property Checking. , 2019, , .		24
4	SoFI: Security Property-Driven Vulnerability Assessments of ICs Against Fault-Injection Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 452-465.	2.7	22
5	Security Beyond CMOS: Fundamentals, Applications, and Roadmap. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3420-3433.	3.1	19
6	FPGA Bitstream Security: A Day in the Life. , 2019, , .		15
7	EMFORCED: EM-Based Fingerprinting Framework for Remarked and Cloned Counterfeit IC Detection Using Machine Learning Classification. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 363-375.	3.1	15
8	A pair selection algorithm for robust RO-PUF against environmental variations and aging. , 2015, , .		14
9	Interconnect-Based PLUF With Signature Uniqueness Enhancement. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 339-352.	3.1	13
10	Reliability vs. security: Challenges and opportunities for developing reliable and secure integrated circuits. , 2016, , .		11
11	Hardware-Assisted Cybersecurity for IoT Devices. , 2017, , .		11
12	Device attestation: Past, present, and future. , 2018, , .		7
13	FLATS: Filling Logic and Testing Spatially for FPGA Authentication and Tamper Detection. , 2019, , .		6
14	ACED-IT: Assuring Confidential Electronic Design Against Insider Threats in a Zero-Trust Environment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3202-3215.	2.7	5
15	SeRFI: Secure Remote FPGA Initialization in an Untrusted Environment. , 2020, , .		4
16	BOFT: Exploitable Buffer Overflow Detection by Information Flow Tracking. , 2021, , .		4
17	Poly-Si-Based Physical Unclonable Functions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 3207-3217.	3.1	3
18	Selective Enhancement of Randomness at the Materials Level: Poly-Si Based Physical Unclonable Functions (PUFs). , 2016, , .		2

#	ARTICLE	IF	CITATIONS
19	AutoMap: Automated Mapping of Security Properties Between Different Levels of Abstraction in Design Flow. , 2021, , .		2
20	Harnessing Nanoscale Device Properties for Hardware Security. , 2015, , .		0