Weichen Liu

List of Publications by Year
in descending order

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124 papers	1,853 citations	394421 19 h-index	434195 31 g-index
124 all docs	124 docs citations	124 times ranked	1342 citing authors

#	Article	IF	Citations
1	FAT: An In-Memory Accelerator With Fast Addition for Ternary Weight Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 781-794.	2.7	2
2	SurgeNAS: A Comprehensive Surgery on Hardware-Aware Differentiable Neural Architecture Search. IEEE Transactions on Computers, 2023, 72, 1081-1094.	3.4	2
3	Solving Dynamic Multiobjective Problem via Autoencoding Evolutionary Search. IEEE Transactions on Cybernetics, 2022, 52, 2649-2662.	9.5	36
4	Designing Efficient DNNs via Hardware-Aware Neural Architecture Search and Beyond. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1799-1812.	2.7	5
5	CARTAD: Compiler-Assisted Reinforcement Learning for Thermal-Aware Task Scheduling and DVFS on Multicores. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1813-1826.	2.7	2
6	EDLAB: A Benchmark for Edge Deep Learning Accelerators. IEEE Design and Test, 2022, 39, 8-17.	1.2	6
7	ArSMART: An Improved SMART NoC Design Supporting Arbitrary-Turn Transmission. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1316-1329.	2.7	6
8	O-Star: An Optical Switching Architecture Featuring Mode and Wavelength-Division Multiplexing for On-Chip Many-Core Systems. Journal of Lightwave Technology, 2022, 40, 24-36.	4.6	14
9	Bringing AI to edge: From deep learningâ€™s perspective. Neurocomputing, 2022, 485, 297-320.	5.9	44
10	HACScale: Hardware-Aware Compound Scaling for Resource-Efficient DNNs. , 2022, , .		0
11	Contention-Aware Routing for Thermal-Reliable Optical Networks-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 260-273.	2.7	10
12	Novel High-Frequency Isolated Cascade PV Inverter Topology Based on Multibus DC Collection. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9, 2122-2135.	5.4	6
13	A Novel Three-Phase Dual-Output Neutral-Point-Clamped Three-Level Inverter. IEEE Transactions on Power Electronics, 2021, 36, 7576-7586.	7.9	13
14	Priority Assignment on Partitioned Multiprocessor Systems With Shared Resources. IEEE Transactions on Computers, 2021, 70, 1006-1018.	3.4	6
15	Reduced Worst-Case Communication Latency Using Single-Cycle Multihop Traversal Network-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1381-1394.	2.7	11
16	A highly sensitive strain sensor based on a silica@polyaniline coreâ€“shell particle reinforced hydrogel with excellent flexibility, stretchability, toughness and conductivity. Soft Matter, 2021, 17, 2142-2150.	2.7	32
17	Efficient AUTOSAR-Compliant CAN-FD Frame Packing with Observed Optimality. , 2021, , .		1
18	HSCoNAS: Hardware-Software Co-Design of Efficient DNNs via Neural Architecture Search. , 2021, , .		6

#	Article	IF	Citations
19	Partial order based non-preemptive communication scheduling towards real-time networks-on-chip. , 2021, , .		4
20	Attack Mitigation of Hardware Trojans for Thermal Sensing via Micro-ring Resonator in Optical NoCs. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-23.	2.3	2
21	Parallel Multipath Transmission for Burst Traffic Optimization in Point-to-Point NoCs. , 2021, , .		1
22	MARCO: A High-performance Task M apping a nd R outing Co -optimization Framework for Point-to-Point NoC-based Heterogeneous Computing Systems. Transactions on Embedded Computing Systems, 2021, 20, 1-21.	2.9	1
23	ZeroBN: Learning Compact Neural Networks For Latency-Critical Edge Systems. , 2021, , .		7
24	Fault-Tolerant Routing Mechanism in 3D Optical Network-on-Chip Based on Node Reuse. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 547-564.	5.6	44
25	Thermal-Aware Design and Simulation Approach for Optical NoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2384-2395.	2.7	7
26	Autonomous temperature sensing for optical network-on-chip. Journal of Systems Architecture, 2020, 102, 101650.	4.3	2
27	Vortex-Assisted Liquid-Liquid Microextraction Based on a Hydrophobic Deep Eutectic Solvent for the Highly Efficient Determination of Sudan I in Food Samples. Analytical Letters, 2020, 53, 1204-1217.	1.8	23
28	Epoxy-based ionic liquid towards multi-walledâ€‚carbonâ€‚nanotubes/polybutylene terephthalate composite with excellent dispersion and conductivity behaviors. Journal of Polymer Research, 2020, 27, 1.	2.4	4
29	Mitigation of Tampering Attacks for MR-Based Thermal Sensing in Optical NoCs. , 2020, , .		3
30	Phase-Locked Strategy of Photovoltaic Connected to Distribution Network With High Proportion Electric Arc Furnace. IEEE Access, 2020, 8, 86012-86023.	4.2	8
31	The thiol group modified multi-wall carbon nanotubes to enhance the dielectric properties of polystyrene. Journal of Polymer Research, 2020, 27, 1.	2.4	6
32	Person Re-Identification Via Pose-Aware Multi-Semantic Learning. , 2020, , .		6
33	Lightweight Thermal Monitoring in Optical Networks-on-Chip via Router Reuse. , 2020, , .		2
34	Scope-Aware Useful Cache Block Calculation for Cache-Related Pre-Emption Delay Analysis With Set-Associative Data Caches. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2333-2346.	2.7	1
35	Contention Minimized Bypassing in SMART NoC. , 2020, , .		6
36	Control Strategy for Four-Leg Nine-Switch Inverter Under Unbalanced Loads. IEEE Access, 2020, 8, 50377-50389.	4.2	6

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37	Tailored Ionic Liquids Encapsulation Method Endowing Hydrogels with Excellent Mechanical and Catalytic Activity. ACS Sustainable Chemistry and Engineering, 2020, 8, 5975-5984.	6.7	22
38	Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence. , 2020, , .		22
39	XOR-Net: An Efficient Computation Pipeline for Binary Neural Network Inference on Edge Devices. , 2020, , .		8
40	EdgeNAS: Discovering Efficient Neural Architectures for Edge Systems. , 2020, , .		6
41	COSMA: An Efficient Concurrency-Oriented Space Management Scheme for In-memory File Systems. , 2020, , .		0
42	Optimal Application Mapping and Scheduling for Network-on-Chips with Computation in STT-RAM Based Router. IEEE Transactions on Computers, 2019, 68, 1174-1189.	3.4	8
43	CASS: Criticality-Aware Standby-Sparing for real-time systems. Journal of Systems Architecture, 2019, 100, 101661.	4.3	4
44	WDM-MDM Silicon-Based Optical Switching for Data Center Networks. , 2019, , .		10
45	Response Time Bounds for Typed DAG Parallel Tasks on Heterogeneous Multi-Cores. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 2567-2581.	5.6	21
46	Routing in optical network-on-chip. , 2019, , .		7
47	NV-eCryptfs: Accelerating Enterprise-Level Cryptographic File System with Non-Volatile Memory. IEEE Transactions on Computers, 2019, 68, 1338-1352.	3.4	5
48	Dynamic No-Fly Zone for Drones. , 2019, , .		2
49	HolyLight: A Nanophotonic Accelerator for Deep Learning in Data Centers. , 2019, , .		41
50	Design of a Hierarchical Clos-Benes Optical Network-on-Chip Architecture. , 2019, , .		1
51	Thermal Sensing Using Micro-ring Resonators in Optical Network-on-Chip. , 2019, , .		6
52	Towards Fast and Lightweight Checkpointing for Mobile Virtualization Using NVRAM. IEEE Transactions on Parallel and Distributed Systems, 2019, 30, 1421-1433.	5.6	0
53	A hydrophobic deep eutectic solvent based vortex-assisted liquid-liquid microextraction for the determination of formaldehyde from biological and indoor air samples by high performance liquid chromatography. Journal of Chromatography A, 2019, 1589, 39-46.	3.7	54
54	Leaking your engine speed by spectrum analysis of real-Time scheduling sequences. Journal of Systems Architecture, 2019, 97, 455-466.	4.3	8

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55	A hydrophobic deep eutectic solventâ€based vortexâ€assisted dispersive liquidâ€“liquid microextraction combined with HPLC for the determination of nitrite in water and biological samples. Journal of Separation Science, 2019, 42, 574-581.	2.5	54
56	Energy-Efficient Application Mapping and Scheduling for Lifetime Guaranteed MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1-14.	2.7	10
57	Hardware-Software Collaborative Thermal Sensing in Optical Network-on-Chip--based Manycore Systems. Transactions on Embedded Computing Systems, 2019, 18, 1-24.	2.9	6
58	TripImputor: Real-Time Imputing Taxi Trip Purpose Leveraging Multi-Sourced Urban Data. IEEE Transactions on Intelligent Transportation Systems, 2018, 19, 3292-3304.	8.0	128
59	A Systematic and Realistic Network-on-Chip Traffic Modeling and Generation Technique for Emerging Many-Core Systems. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 113-126.	2.4	6
60	Fine-Grained Task-Level Parallel and Low Power H.264 Decoding in Multi-Core Systems. , 2018, , .		2
61	User Experience-Enhanced and Energy-Efficient Task Scheduling on Heterogeneous Multi-Core Mobile Systems. , 2018, , .		1
62	Work-in-Progress: Communication Optimization for Thermal Reliable Optical Network-on-Chip. , 2018, , .		0
63	Analyzing Data Cache Related Preemption Delay With Multiple Preemptions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2255-2265.	2.7	5
64	ACA-SDS: Adaptive Crypto Acceleration for Secure Data Storage in Big Data. IEEE Access, 2018, 6, 44494-44505.	4.2	4
65	Thermal-Aware Task Mapping on Dynamically Reconfigurable Network-on-Chip Based Multiprocessor System-on-Chip. IEEE Transactions on Computers, 2018, 67, 1818-1834.	3.4	32
66	An Efficient UAV Hijacking Detection Method Using Onboard Inertial Measurement Unit. Transactions on Embedded Computing Systems, 2018, 17, 1-19.	2.9	29
67	Dark silicon-aware hardware-software collaborated design for heterogeneous many-core systems. , 2017, , .		7
68	Quantitative Modeling of Thermo-Optic Effects in Optical Networks-on-Chip. , 2017, , .		7
69	Task Mapping on SMART NoC. , 2017, , .		29
70	Efficient drone hijacking detection using onboard motion sensors. , 2017, , .		26
71	FoToNoC: A Folded Torus-Like Network-on-Chip Based Many-Core Systems-on-Chip in the Dark Silicon Era. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 1905-1918.	5.6	26
72	Fixed priority scheduling of real-time flows with arbitrary deadlines on smart NoCs. , 2017, , .		5

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73	Hardware-software collaboration for dark silicon heterogeneous many-core systems. Future Generation Computer Systems, 2017, 68, 234-247.	7.5	9
74	Communication optimization for thermal reliable many-core systems. , 2017, , .		1
75	Chip Temperature Optimization for Dark Silicon Many-Core Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	11
76	FoToNoC: A hierarchical management strategy based on folded torus-like Network-on-Chip for dark silicon many-core systems. , 2016, , .		9
77	An Efficient Technique of Application Mapping and Scheduling on Real-Time Multiprocessor Systems for Throughput Optimization. Transactions on Embedded Computing Systems, 2016, 15, 1-25.	2.9	3
78	Through Global Sharing to Improve Network Efficiency for Radio-Frequency Interconnect Based Network-on-Chip. IEEE Access, 2016, 4, 6503-6514.	4.2	0
79	Thermal-Aware Task Scheduling for 3D-Network-on-Chip: A Bottom to Top Scheme. Journal of Circuits, Systems and Computers, 2016, 25, 1640003.	1.5	8
80	ApproxMap: On task allocation and scheduling for resilient applications. , 2016, , .		5
81	Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3027-3040.	3.1	31
82	Distributed Sensor Network-on-Chip for Performance Optimization of Soft-Error-Tolerant Multiprocessor System-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1546-1559.	3.1	9
83	nCode: Limiting Harmful Writes to Emerging Mobile NVRAM through Code Swapping. , 2015, , .		4
84	Realistic Task Parallelization of the H.264 Decoding Algorithm for Multiprocessors. , 2015, , .		1
85	Efficient SAT-based application mapping and scheduling on multiprocessor systems for throughput maximization. , 2015, , .		4
86	An Efficient Technique for Chip Temperature Optimization of Multiprocessor Systems in the Dark Silicon Era. , 2015, , .		5
87	User Experience Enhanced Task Scheduling and Processor Frequency Scaling for Energy-Sensitive Mobile Devices. , 2015, , .		2
88	Traffic-Aware Application Mapping for Network-on-Chip Based Multiprocessor System-on-Chip. , 2015, , .		8
89	Isolation of Physical and Logical Views of Dark-Silicon Many-Core Systems for Reliability and Performance Co-Optimization. Communications in Computer and Information Science, 2015, , 99-109.	0.5	0
90	A systematic network-on-chip traffic modeling and generation methodology. , 2014, , .		4

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91	DR. Swap. , 2014, , .		25
92	Building high-performance smartphones via non-volatile memory. , 2014, , .		42
93	Enhancing lifetime of NVM-based main memory with bit shifting and flipping. , 2014, , .		6
94	On-chip sensor networks for soft-error tolerant real-time multiprocessor systems-on-chip. ACM Journal on Emerging Technologies in Computing Systems, 2014, 10, 1-20.	2.3	2
95	Thermal-aware task scheduling for 3D-network-on-chip: A Bottom-to-Top scheme. , 2014, , .		2
96	UNION: A Unified Inter/Intrachip Optical Network for Chip Multiprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1082-1095.	3.1	13
97	Contention-aware task and communication co-scheduling for network-on-chip based Multiprocessor System-on-Chip. , 2014, , .		0
98	A Case Study on the Communication and Computation Behaviors of Real Applications in NoC-Based MPSoCs. , 2014, , .		34
99	An Improved Thermal Model for Static Optimization of Application Mapping and Scheduling in Multiprocessor System-on-Chip. , 2014, , .		8
100	Formal Worst-Case Analysis of Crosstalk Noise in Mesh-Based Optical Networks-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1823-1836.	3.1	69
101	On-Chip Sensor Network for Efficient Management of Power Gating-Induced Power/Ground Noise in Multiprocessor System on Chip. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 767-777.	5.6	4
102	System-Level Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 292-305.	3.1	38
103	3-D Mesh-Based Optical Network-on-Chip for Multiprocessor System-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 584-596.	2.7	93
104	A Torus-Based Hierarchical Optical-Electronic Network-on-Chip for Multiprocessor System-on-Chip. ACM Journal on Emerging Technologies in Computing Systems, 2012, 8, 1-26.	2.3	52
105	A novel low-waveguide-crossing floorplan for fat tree based optical networks-on-chip. , 2012, , .		0
106	Thermal analysis for 3D optical network-on-chip based on a novel low-cost 6×6 optical router. , 2012, , .		3
107	An efficient soft error protection scheme for MPSoC and FPGA-based verification. , 2012, , .		1
108	Satisfiability Modulo Graph Theory for Task Mapping and Scheduling on Multiprocessor Systems. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 1382-1389.	5.6	35

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109	A NoC Traffic Suite Based on Real Applications. , 2011, , .		85
110	Modeling and Analysis of Thermal Effects in Optical Networks-on-Chip. , 2011, , .		12
111	A Hardware-Software Collaborated Method for Soft-Error Tolerant MPSoC. , 2011, , .		6
112	Power Gating Aware Task Scheduling in MPSoC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1801-1812.	3.1	11
113	Coroutine-Based Synthesis of Efficient Embedded Software From SystemC Models. IEEE Embedded Systems Letters, 2011, 3, 46-49.	1.9	1
114	Crosstalk noise and bit error rate analysis for optical network-on-chip. , 2010, , .		95
115	A Hierarchical Hybrid Optical-Electronic Network-on-Chip. , 2010, , .		50
116	UNION: A unified inter/intra-chip optical network for chip multiprocessors. , 2010, , .		12
117	An efficient technique for analysis of minimal buffer requirements of synchronous dataflow graphs with model checking. , 2009, , .		21
118	Efficient algorithms for 2D area management and online task placement on runtime reconfigurable FPGAs. Microprocessors and Microsystems, 2009, 33, 374-387.	2.8	4
119	On-line MPSoC Scheduling Considering Power Gating Induced Power/Ground Noise. , 2009, , .		9
120	Efficient Software Synthesis for Dynamic Single Appearance Scheduling of Synchronous Dataflow. IEEE Embedded Systems Letters, 2009, 1, 69-72.	1.9	3
121	A case study of on-chip sensor network in multiprocessor system-on-chip. , 2009, , .		4
122	Efficient SAT-Based Mapping and Scheduling of Homogeneous Synchronous Dataflow Graphs for Throughput Optimization. , 2008, , .		37
123	An Efficient Algorithm for Online Soft Real-Time Task Placement on Reconfigurable Hardware Devices. , 2007, , .		19
124	Improved Schedulability Analysis of EDF Scheduling on Reconfigurable Hardware Devices. , 2007, , .		6