Hisashi Kino

List of Publications by Year
in descending order

68	319	1163117 8	1125743 13
papers	citations	h-index	g-index

68	68	68	161
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Room-Temperature Cu Direct Bonding Technology Enabling 3D Integration with Micro-LEDs. , 2022, , .		5
2	Wafer-Level Flexible 3D Corrugated Interconnect Formation for Scalable In-Mold Electronics with Embedded Chiplets. , 2021, , .		2
3	Development of Manganese Nitride Resistor with Near-Zero Temperature-Coefficient of Resistance to Achieve High-Thermal-Stability ICs. , 2021, , .		2
4	High-thermal-stability resistor formed from manganese nitride compound that exhibits the saturation state of the mean free path. Applied Physics Express, 2021, 14, 091003.	2.4	3
5	Integration of Damage-less Probe Cards Using Nano-TSV Technology for Microbumped Wafer Testing. , 2021, , .		4
6	Design and Evaluation of Electronic-Microsaccade with Balanced Stimulation for Artificial Vision System. , 2021, , .		1
7	Multichip thinning technology with temporary bonding for multichip-to-wafer 3D integration. Japanese Journal of Applied Physics, 2020, 59, SBBA04.	1.5	3
8	Symmetric and asymmetric spike-timing-dependent plasticity function realized in a tunnel-field-effect-transistor-based charge-trapping memory. Japanese Journal of Applied Physics, 2020, 59, SGGB12.	1.5	2
9	Generation of STDP With Non-Volatile Tunnel-FET Memory for Large-Scale and Low-Power Spiking Neural Networks. IEEE Journal of the Electron Devices Society, 2020, 8, 1266-1271.	2.1	3
10	Low-temperature multichip-to-wafer 3D integration based on via-last TSV with OER-TEOS-CVD and microbump bonding without solder extrusion. , 2020, , .		2
11	RDL-first Flexible FOWLP Technology with Dielets Embedded in Hydrogel. , 2020, , .		5
12	Significant Die-Shift Reduction and Î¼LED Integration Based on Die-First Fan-Out Wafer-Level Packaging for Flexible Hybrid Electronics. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2020, 10, 1419-1422.	2.5	5
13	7-Î¼m-thick NCF technology with low-height solder microbump bonding for 3D integration. , 2020, , .		2
14	Development of Non-Volatile Tunnel-FET Memory as a Synaptic Device for Low-Power Spiking Neural Networks. , 2020, , .		1
15	<scp>Onâ€wafer</scp> thermomechanical characterization of a thin film polyimide formed by vapor deposition polymerization for <scp>throughâ€silicon</scp> via applications: Comparison to <scp>plasmaâ€enhanced</scp> chemical vapor deposition <scp>SiO₂</scp>. Journal of Polymer Science, 2020, 58, 2248-2258.	3.8	5
16	Mechanical Characterization of FOWLPBased Flexible Hybrid Electronics (FHE) for Biomedical Sensor Application. , 2019, , .		0
17	Mechanical and Electrical Characterization of FOWLP-Based Flexible Hybrid Electronics (FHE) for Biomedical Sensor Application. , 2019, , .		6
18	Investigation of TSV Liner Interface With Multiwell Structured TSV to Suppress Noise Propagation in Mixed-Signal 3D-IC. IEEE Journal of the Electron Devices Society, 2019, 7, 1225-1231.	2.1	6

#	Article	IF	Citations
19	Noise Propagation through TSV in Mixed-Signal 3D-IC and Investigation of Liner Interface with Multi-Well Structured TSV. , 2019, , .		1
20	Development of Eccentric Spin Coating of Polymer Liner for Low-Temperature TSV Technology With Ultra-Fine Diameter. IEEE Electron Device Letters, 2019, 40, 95-98.	3.9	14
21	The Effect of Tungsten Volume on Residual Stress and Cell Characteristics in MONOS. IEEE Journal of the Electron Devices Society, 2019, 7, 382-387.	2.1	2
22	Investigation of the Impact of External Stress on Memory Characteristics by Modifying the Backside of Substrate. IEEE Transactions on Electron Devices, 2019, 66, 1741-1746.	3.0	1
23	Investigation of the Underfill with Negative-Thermal-Expansion Material to Suppress Mechanical Stress in 3D Integration System. , 2019, , .		1
24	PPG and SpO₂ Recording Circuit with Ambient Light Cancellation for Trans-Nail Pulse-Wave Monitoring System. , 2019, , .		5
25	Characterization of Low-Height Solder Microbump Bonding for Fine-Pitch Inter-Chip Connection in 3DICs. , 2019, , .		2
26	Impacts of Deposition Temperature and Annealing Condition on Ozone-Ethylene Radical Generation-TEOS-CVD SiO2 for Low-Temperature TSV Liner Formation. , 2019, , .		0
27	Multichip thinning technology with temporary bonding for multichip-to-wafer 3D integration. , 2019, , .		0
28	Development of 3D-IC Embedded Flexible Hybrid System. , 2019, , .		2
29	Development of a CDS Circuit for 3-D Stacked Neural Network Chip using CMOS Analog Signal Processing. , 2019, , .		0
30	High-Thermoresistant Temporary Bonding Technology for Multichip-to-Wafer 3-D Integration With Via-Last TSVs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 181-188.	2.5	5
31	Development of integrated photoplethysmographic recording circuit for trans-nail pulse-wave monitoring system. Japanese Journal of Applied Physics, 2018, 57, 04FM11.	1.5	6
32	Tunnel field-effect transistor charge-trapping memory with steep subthreshold slope and large memory window. Japanese Journal of Applied Physics, 2018, 57, 04FE07.	1.5	6
33	Process Integration for FlexTrate^{TM}. , 2018, , .		2
34	Continuous Peripheral Blood Pressure Measurement with ECG and PPG Signals at Fingertips. , 2018, , .		3
35	The Effect of Mechanical Stress on Cell Characteristics in MONOS Structures. IEEE Transactions on Electron Devices, 2018, 65, 4313-4319.	3.0	4
36	Charge-Trap-Free Polymer-Liner Through-Silicon Vias for Reliability Improvement of 3D ICs. , 2018, , .		6

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37	Self-Assembly Technologies for FlexTrateâ„¢. , 2018, , .		6
38	Study of Al-doped ZnO Transparent Stimulus Electrode for Fully Implantable Retinal Prosthesis with Three-dimensionally Stacked Retinal Prosthesis Chip. Sensors and Materials, 2018, , 225.	0.5	6
39	Evaluation of insertion characteristics of less invasive Si optoneural probe with embedded optical fiber. Japanese Journal of Applied Physics, 2017, 56, 04CM08.	1.5	1
40	3-D Sidewall Interconnect Formation Climbing Over Self-Assembled KGDs for Large-Area Heterogeneous Integration. IEEE Transactions on Electron Devices, 2017, 64, 2912-2918.	3.0	5
41	Minimized hysteresis and low parasitic capacitance TSV with PBO (polybenzoxazole) liner to achieve ultra-high-speed data transmission. , 2017, , .		4
42	Ultrawide range square wave impedance analysis circuit with ultra-slow ring-oscillator using gate-induced drain-leakage current. , 2017, , .		0
43	Design and evaluation of wide-range and low-power analog front-end enabling body-implanted devices to monitor charge injection properties. Japanese Journal of Applied Physics, 2017, 56, 04CM05.	1.5	0
44	Development of Si neural probe with piezoresistive force sensor for minimally invasive and precise monitoring of insertion forces. Japanese Journal of Applied Physics, 2017, 56, 04CM04.	1.5	0
45	Self-Assembly and Electrostatic Carrier Technology for Via-Last TSV Formation Using Transfer Stacking-Based Chip-to-Wafer 3-D Integration. IEEE Transactions on Electron Devices, 2017, 64, 5065-5072.	3.0	11
46	Experimental evaluation of stimulus current generator with Laplacian edge-enhancement for 3-D stacked retinal prosthesis chip. , 2017, , .		6
47	Remarkable Suppression of Local Stress in 3D IC by Manganese Nitride-Based Filler with Large Negative CTE. , 2017, , .		19
48	Evaluation of in-plane local stress distribution in stacked IC chip using dynamic random access memory cell array for highly reliable three-dimensional IC. Japanese Journal of Applied Physics, 2016, 55, 04EC07.	1.5	1
49	Oxide-Oxide Thermocompression Direct Bonding Technologies with Capillary Self-Assembly for Multichip-to-Wafer Heterogeneous 3D System Integration. Micromachines, 2016, 7, 184.	2.9	17
50	Effect of local stress induced by thermal expansion of underfill in three-dimensional stacked IC. Japanese Journal of Applied Physics, 2016, 55, 04EC03.	1.5	8
51	Wide-range and precise tissue impedance analysis circuit with ultralow current source using gate-induced drain-leakage current. , 2016, , .		1
52	Highly sensitive pressure sensor with silicon-on-nothing (SON) MOSFET for sensor integrated heterogeneous system. , 2016, , .		0
53	Design and evaluation of area-efficient and wide-range impedance analysis circuit for multichannel high-quality brain signal recording system. Japanese Journal of Applied Physics, 2016, 55, 04EM12.	1.5	4
54	Drastic reduction of keep-out-zone in 3D-IC by local stress suppression with negative-CTE filler. , 2016, , .		1

#	Article	IF	Citations
55	Impact of Chip-Edge Structures on Alignment Accuracies of Self-Assembled Dies for Microelectronic System Integration. Journal of Microelectromechanical Systems, 2016, 25, 91-100.	2.5	9
56	Consideration of microbump layout for reduction of local bending stress due to CTE Mismatch in 3D IC. , 2015, , .		2
57	Impact of deep-via plasma etching process on transistor performance in 3D-IC with via-last backside TSV. , 2015, , .		2
58	Novel local stress evaluation method in 3D IC using DRAM cell array with planar mOS capacitors. , 2015, , .		1
59	Vertical-cavity surface-emitting laser chip bonding by surface-tension-driven self-assembly for optoelectronic heterogeneous integration. Japanese Journal of Applied Physics, 2015, 54, 030206.	1.5	8
60	Development of highly-reliable microbump bonding technology using self-assembly of NCF-covered KGDs and multi-layer 3D stacking challenges. , 2015, , .		10
61	Reconfigured-Wafer-to-Wafer 3-D Integration Using Parallel Self-Assembly of Chips With Cuâ€“SnAg Microbumps and a Nonconductive Film. IEEE Transactions on Electron Devices, 2014, 61, 533-539.	3.0	41
62	Deteriorated Device Characteristics in 3D-LSI Caused by Distorted Silicon Lattice. IEEE Transactions on Electron Devices, 2014, 61, 540-547.	3.0	8
63	Minimization of Keep-Out-Zone (KOZ) in 3D IC by local bending stress suppression with low temperature curing adhesive. , 2014, , .		5
64	Investigation of Local Bending Stress Effect on Complementary Metalâ€“Oxideâ€“Semiconductor Characteristics in Thinned Si Chip for Chip-to-Wafer Three-Dimensional Integration. Japanese Journal of Applied Physics, 2013, 52, 04CB11.	1.5	16
65	Fabrication and In vivo Evaluation of Poly(3,4-ethylenedioxythiophene) Stimulus Electrodes for Fully Implantable Retinal Prosthesis. Japanese Journal of Applied Physics, 2013, 52, 04CL03.	1.5	4
66	Study of Insertion Characteristics of Si Neural Probe with Sharpened Tip for Minimally Invasive Insertion to Brain. Japanese Journal of Applied Physics, 2013, 52, 04CL04.	1.5	2
67	HIGH ENDURANCE NON-VOLATILE SEMICONDUCTOR MEMORY FOR FULLY IMPLANTABLE RETINAL PROSTHESIS. , 2012, , .		0
68	MOSFET Nonvolatile Memory with High-Density Cobalt-Nanodots Floating Gate and $hbox{HfO}_{f 2}$ High-k Blocking Dielectric. IEEE Nanotechnology Magazine, 2011, 10, 528-531.	2.0	4