Sai-Weng Sin

List of Publications by Year
in descending order

164 papers	2,248 citations	394421 19 h-index	276875 41 g-index
167 all docs	167 docs citations	167 times ranked	1290 citing authors

#	Article	IF	Citations
1	Background Timing Mismatch Calibration Techniques in High-Speed Time-Interleaved ADCs: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2564-2569.	3.0	0
2	Wideband Continuous-Time MASH Delta-Sigma Modulators: A Tutorial Review. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2623-2628.	3.0	7
3	An FPGA-Based Self-Reconfigurable Arc Fault Detection System for Smart Meters. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 4133-4137.	3.0	2
4	Design of Fast Transient Response Voltage-Mode Buck Converter With Hybrid Feedforward and Feedback Technique. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2021, 9, 780-790.	5.4	13
5	Bird'sâ€eye view of analog and mixedâ€signal chips for the 21st century. International Journal of Circuit Theory and Applications, 2021, 49, 746-761.	2.0	7
6	Discrete-Time MASH Delta-Sigma Modulator with Second-Order Digital Noise Coupling for Wideband High-Resolution Applications. , 2021, , .		7
7	A Time-Interleaved 2nd-Order Î”Î£ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation. IEEE Journal of Solid-State Circuits, 2021, 56, 2375-2387.	5.4	9
8	Recent Advances in High-Resolution Hybrid Discrete-Time Noise-Shaping ADCs. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 129-139.	2.7	4
9	Background Timing-Skew Mismatch Calibration for Time-Interleaved ADCs. , 2021, , .		1
10	Advances in Continuous-time MASH Î”Î£ Modulators. , 2021, , .		0
11	A 95% Peak Efficiency Modified KY (Boost) Converter for IoT with Continuous Flying Capacitor Charging in DCM. , 2021, , .		1
12	Analysis, Design and Control of an Integrated Three-Level Buck Converter under DCM Operation. Journal of Circuits, Systems and Computers, 2020, 29, 2050011.	1.5	0
13	A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration. IEEE Journal of Solid-State Circuits, 2020, 55, 693-705.	5.4	41
14	A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance. IEEE Journal of Solid-State Circuits, 2020, 55, 344-355.	5.4	38
15	LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter With Ripple Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4174-4186.	5.4	6
16	A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved 2nd-Order Î”Î£ Modulator with Digital Feedforward Extrapolation in 28nm CMOS. , 2020, , .		6
17	Digital Battery Management Unit With Built-In Resistance Compensation, Modulated Frequency Detection and Multi-Mode Protection for Fast, Efficient and Safe Charging. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4063-4074.	5.4	3
18	A 5 GS/s 29 mW Interleaved SAR ADC With 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications. IEEE Access, 2020, 8, 138944-138954.	4.2	17

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19	A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter With Seamless Mode Selection for IoT Application. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4085-4098.	5.4	31
20	A SAR-ADC-Assisted DC-DC Buck Converter With Fast Transient Recovery. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1669-1673.	3.0	7
21	Design of KY Converter With Constant On-Time Control Under DCM Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1753-1757.	3.0	11
22	An Integrated DCâ€“DC Converter With Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery. IEEE Journal of Solid-State Circuits, 2019, 54, 2637-2648.	5.4	6
23	A 10b 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration. , 2019, , .		6
24	A 29mW 5GS/s Time-interleaved SAR ADC achieving 48.5dB SNDR With Fully-Digital Timing-Skew Calibration Based on Digital-Mixing. , 2019, , .		14
25	20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH Î”Î£ Modulator with 1.5b/4b Quantizers in 28nm CMOS. , 2019, , .		9
26	Multibit Sturdy MASH Î”Î£ Modulator with Error-shaped Segmented DACs for Wideband Low-power Applications. , 2019, , .		0
27	A High DR High-Input-Impedance Programmable-Gain ECG Acquisition Interface with Non-inverting Continuous Time Sigma-Delta Modulator. , 2019, , .		3
28	Digital Battery Management Unit with Built-In Resistance Compensation and Accidental Mutation Protection for Fast and Accurate Charging. , 2019, , .		2
29	Instantaneous power quality indices detection under frequency deviated environment. IET Science, Measurement and Technology, 2019, 13, 1111-1121.	1.6	12
30	A 550-mu W 20-kHz BW 100.8-dB SNDR Linear- Exponential Multi-Bit Incremental $SigmaDelta$ ADC With 256 Clock Cycles in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 1161-1172.	5.4	45
31	Accuracy-Enhanced Variance-Based Time-Skew Calibration Using SAR as Window Detector. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 481-485.	3.1	10
32	A 1.2V 86dB SNDR 500kHz BW Linear-Exponential Multi-Bit Incremental ADC Using Positive Feedback in 65nm CMOS. , 2019, , .		7
33	Quick and cost-efficient A/D converter static characterization using low-precision testing signal. Microelectronics Journal, 2018, 74, 86-93.	2.0	2
34	Review and Selection Strategy for High-Accuracy Modeling of PWM Converters in DCM. Journal of Electrical and Computer Engineering, 2018, 2018, 1-16.	0.9	6
35	A Power Quality Indexes Measurement System Platform with Remote Alarm Notification. , 2018, , .		4
36	An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery. , 2018, , .		1

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37	A 550ÂµW 20kHz BW 100.8DB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65NM CMOS. , 2018, , .		2
38	Design and Control of An Integrated 3-Level Boost Converter under DCM Operation. , 2018, , .		6
39	A 14-Bit Split-Pipeline ADC With Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1380-1384.	3.0	5
40	A 10-MHz Bandwidth Two-Path Third-Order <inline-formula> <tex-math notation="LaTeX">$SigmaDelta$ </tex-math> </inline-formula> Modulator With Cross-Coupling Branches. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1410-1414.	3.0	3
41	A Reconfigurable and Extendable Digital Architecture for Mixed Signal Power Electronics Controller. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1480-1484.	3.0	4
42	A 220-MHz Bondwire-Based Fully-Integrated KY Converter With Fast Transient Response Under DCM Operation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, , 1-12.	5.4	11
43	Metastablility in SAR ADCs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 111-115.	3.0	15
44	A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 166-170.	3.0	111
45	Activeâ€“Passive $Delta Sigma $ Modulator for High-Resolution and Low-Power Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 364-374.	3.1	20
46	A sub-1V 78-nA bandgap reference with curvature compensation. Microelectronics Journal, 2017, 63, 35-40.	2.0	14
47	DCM operation analysis of 3â€level boost converters. Electronics Letters, 2017, 53, 270-272.	1.0	5
48	A 7.8-mW 5-b 5-GS/s Dual-Edges-Triggered Time-Based Flash ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1966-1976.	5.4	21
49	A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH $Delta Sigma $ Modulator With Multirate Opamp Sharing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2641-2654.	5.4	39
50	A 12b 180MS/s 0.068mm² With Full-Calibration-Integrated Pipelined-SAR ADC. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 1684-1695.	5.4	24
51	Reconfigurable mismatchâ€free timeâ€interleaved bandpass sigmaâ€“delta modulator for wireless communications. Electronics Letters, 2017, 53, 506-508.	1.0	3
52	Split-based time-interleaved ADC with digital background timing-skew calibration. , 2017, , .		5
53	A digital PWM controlled KY step-up converter based on passive sigma-delta modulator. , 2017, , .		2
54	A digital PWM controlled KY step-up converter based on frequency domain Î£Î” ADC. , 2017, , .		1

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55	Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial $V_{mathrm {cm}}$ -Based Switching. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1168-1172.	3.1	12
56	CCM operation analysis and parameters design of Negative Output Elementary Luo Converter for ripple suppression. , 2017, , .		1
57	A 5-bit 2 GS/s binary-search ADC with charge-steering comparators. , 2017, , .		1
58	A high DR multi-channel stage-shared hybrid front-end for integrated power electronics controller. , 2016, , .		7
59	A high resolution multi-bit incremental converter insensitive to DAC mismatch error. , 2016, , .		6
60	A 94-dB DR,105-Hz bandwidth interface circuit for inertial navigation applications. , 2016, , .		0
61	An 8-bit 0.7-GS/s single channel flash-SAR ADC in 65-nm CMOS technology. , 2016, , .		7
62	A 12b 180MS/s 0.068mm² pipelined-SAR ADC with merged-residue DAC for noise reduction. , 2016, , .		4
63	Limit Cycle Oscillation Reduction for Digital Low Dropout Regulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 903-907.	3.0	49
64	A Fully Integrated Digital LDO With Coarseâ€“Fine-Tuning and Burst-Mode Operation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 683-687.	3.0	116
65	A 6 b 5 GS/s 4 Interleaved 3 b/Cycle SAR ADC. IEEE Journal of Solid-State Circuits, 2016, 51, 365-377.	5.4	32
66	Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2603-2607.	3.1	14
67	A 4x Time-Domain Interpolation 6-bit 3.4 GS/s 12.6 mW Flash ADC in 65 nm CMOS. Journal of Semiconductor Technology and Science, 2016, 16, 395-404.	0.4	1
68	Generalized Type III controller design interface for DC-DC converters. , 2015, , .		0
69	Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 537-547.	3.6	8
70	Capacitive floating level shifter: Modeling and design. , 2015, , .		3
71	20.4 A 123-phase DC-DC converter-ring with fast-DVS for microprocessors. , 2015, , .		35
72	DCM operation analysis of KY converter. Electronics Letters, 2015, 51, 2037-2039.	1.0	9

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73	A 89fJ-FOM 6-bit 3.4GS/s flash ADC with 4x time-domain interpolation. , 2015, , .		14
74	Self-Reconfiguration Property of a Mixed Signal Controller for Improving Power Quality Compensation During Light Loading. IEEE Transactions on Power Electronics, 2015, 30, 5938-5951.	7.9	11
75	A review and design of the on-chip rectifiers for RF energy harvesting. , 2015, , .		28
76	26.5 A 5.5mW 6b 5GS/S 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS. , 2015, , .		12
77	Resolutionâ€enhanced sturdy MASH deltaâ€“sigma modulator for wideband lowâ€voltage applications. Electronics Letters, 2015, 51, 1061-1063.	1.0	9
78	Thermal and Reference Noise Analysis of Time-Interleaving SAR and Partial-Interleaving Pipelined-SAR ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2196-2206.	5.4	21
79	Time interleaved current steering DAC for ultra-high conversion rate. , 2014, , .		3
80	Jitter-resistant Capacitor Based Sine-Shaped DAC for Continuous-Time Sigma-Delta modulators. , 2014, , .		1
81	Split-SAR ADCs: Improved Linearity With Power and Speed Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 372-383.	3.1	53
82	A 0.6V 8b 100MS/s SAR ADC with minimized DAC capacitance and switching energy in 65nm CMOS. , 2013, , .		4
83	Excess-loop-delay compensation technique for CT Î”Î£ modulator with hybrid activeâ€“passive loop-filters. Analog Integrated Circuits and Signal Processing, 2013, 76, 35-46.	1.4	0
84	A continuous-time VCO-assisted VCO-based ΣΔ modulator with 76.6dB SNDR and 10MHz BW. , 2013, , .		1
85	A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 2154-2169.	5.4	18
86	A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration. , 2013, , .		1
87	A background gain- calibration technique for low voltage pipelined ADCs based on nonlinear interpolation. , 2013, , .		2
88	A 2.3 mW 10-bit 170 MS/s Two-Step Binary-Search Assisted Time-Interleaved SAR ADC. IEEE Journal of Solid-State Circuits, 2013, 48, 1783-1794.	5.4	34
89	An ELD tracking compensation technique for active-RC CT ΣΔ modulators. , 2012, , .		0
90	A 34fJ 10b 500 MS/s partial-interleaving pipelined SAR ADC. , 2012, , .		20

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91	A 50-fJ 10-b 160-MS/s Pipelined-SAR ADC Decoupled Flip-Around MDAC and Self-Embedded Offset Cancellation. IEEE Journal of Solid-State Circuits, 2012, 47, 2614-2626.	5.4	27
92	A 2.3mW 10-bit 170MS/s two-step binary-search assisted time-interleaved SAR ADC. , 2012, , .		8
93	A 10MHz BW 78dB DR CT ΣΔ modulator with novel switched high linearity VCO-based quantizer. , 2012, , .		1
94	Inter-Stage Gain Error self-calibration of a 31.5fJ 10b 470MS/S Pipelined-SAR ADC. , 2012, , .		5
95	A 0.024 mm² 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS. , 2012, , .		2
96	A DT 0â€“2 MASH Î£Î” modulator with VCO-based quantizer for enhanced linearity. , 2012, , .		0
97	An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC. IEEE Journal of Solid-State Circuits, 2012, 47, 2763-2772.	5.4	78
98	A 3.8mW 8b 1GS/s 2b/cycle interleaving SAR ADC with compact DAC structure. , 2012, , .		15
99	A 10-bit SAR ADC with two redundant decisions and splitted-MSB-cap DAC array. , 2012, , .		2
100	A 22.4 μW 80dB SNDR ΣΔ modulator with passive analog adder and SAR quantizer for EMG application. , 2012, , .		8
101	A robust NTF zero optimization technique for both low and high OSRs sigma-delta modulators. , 2012, , .		2
102	A 12-bit 110MS/s 4-stage single-opamp pipelined SAR ADC with ratio-based GEC technique. , 2012, , .		6
103	A nonlinearity digital background calibration algorithm for 2.5bit/stage pipelined ADCs with opamp sharing architecture. , 2011, , .		0
104	A 7-bit 300-MS/s subranging ADC with embedded threshold & gain-loss calibration. , 2011, , .		1
105	Hybrid loopfilter sigma-delta modulator with NTF zero compensation. , 2011, , .		4
106	Design techniques for nanometer wideband power-efficient CMOS ADCs. , 2011, , .		0
107	A FPGA-based power electronics controller for hybrid active power filters. , 2011, , .		5
108	NTF zero compensation technique for passive sigma-delta modulator. , 2011, , .		3

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109	A 4.8-bit ENOB 5-bit 500MS/s binary-search ADC with minimized number of comparators. , 2011, , .		13
110	A 0.024mm² 8b 400MS/s SAR ADC with 2b/cycle and resistive DAC in 65nm CMOS. , 2011, , .		31
111	Multi-merged-switched redundant capacitive DACs for 2b/cycle SAR ADC. , 2011, , .		0
112	A 35 fJ 10b 160 MS/s pipelined-SAR ADC with decoupled flip-around MDAC and self-embedded offset cancellation. , 2011, , .		12
113	Noise shaping implementation in two-step/SAR ADC architectures based on delayed quantization error. , 2011, , .		5
114	A time-efficient dither-injection scheme for pipelined SAR ADC. , 2011, , .		1
115	A charge pump based timing-skew calibration for time-interleaved ADC. , 2011, , .		0
116	Clock-jitter sensitivity reduction in CT ΣΔ modulators using voltage-crossing detection DAC. , 2011, , .		0
117	A dual-VCO-based quantizer with highly improved linearity and enlarged dynamic range. , 2011, , .		3
118	A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS. , 2011, , .		40
119	A passive Excess-Loop-Delay compensation technique for Gm-C based continuous-time ΣΔ modulators. , 2011, , .		4
120	FPGA-based decoupled double synchronous reference frame PLL for active power filters. , 2011, , .		9
121	Linearity Analysis on a Series-Split Capacitor Array for High-Speed SAR ADCs. VLSI Design, 2010, 2010, 1-8.	0.5	9
122	A threshold-embedded offset calibration technique for inverter-based flash ADCs. , 2010, , .		6
123	A power effective 5-bit 600 MS/s binary-search ADC with simplified switching. , 2010, , .		7
124	A voltage feedback charge compensation technique for split DAC architecture in SAR ADCs. , 2010, , .		7
125	Parasitics nonlinearity cancellation technique for split DAC architecture by using capacitive charge-pump. , 2010, , .		5
126	Design and Experimental Verification of a Power Effective Flash-SAR Subranging ADC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 607-611.	3.0	28

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127	A Rapid Power-Switchable Track-and-Hold Amplifier in 90-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 16-20.	3.0	17
128	A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2010, 45, 1111-1121.	5.4	571
129	Level-Shifting variable current charging technique for high-speed Comparator-Based Switched-Capacitor circuits. , 2010, , .		1
130	An ultra low power 9-bit 1-MS/s pipelined SAR ADC for bio-medical applications. , 2010, , .		1
131	A Fixed-Pulse Shape Feedback Technique with reduced clock-jitter sensitivity in Continuous-Time sigma-delta modulators. , 2010, , .		2
132	An efficient DAC and interstage gain error calibration technique for multi-bit pipelined ADCs. , 2010, , .		2
133	A reduced jitter-sensitivity clock generation technique for continuous-time ΣΔ modulators. , 2010, , .		0
134	A process-insensitive current-controlled delay generator with threshold voltage compensation. , 2010, , .		0
135	A background amplifier offset calibration technique for high-resolution pipelined ADCs. , 2010, , .		4
136	An 11b 60MS/s 2.1mW two-step time-interleaved SAR-ADC with reused S&H. , 2010, , .		11
137	A digital background nonlinearity calibration algorithm for pipelined ADCs. , 2010, , .		1
138	Advanced Low Voltage Circuit Techniques. , 2010, , 27-54.		0
139	Design of a 1.2 V, 10-bit, 60â€“360 MHz Time-Interleaved Pipelined ADC. , 2010, , 75-95.		0
140	Challenges in Low-Voltage Circuit Designs. , 2010, , 11-26.		0
141	Experimental Results. , 2010, , 97-112.		0
142	Conclusions and Prospective for Future Work. , 2010, , 113-116.		0
143	A voltage-controlled capacitance offset calibration technique for high resolution dynamic comparator. , 2009, , .		13
144	Parasitic calibration by two-step ratio approaching technique for split capacitor array SAR ADCs. , 2009, , .		4

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145	A modified charging algorithm for comparator-based switched-capacitor circuits. , 2009, , .		3
146	On-chip small capacitor mismatches measurement technique using beta-multiplier-biased ring oscillator. , 2009, , .		7
147	Comparator-based successive folding ADC. , 2009, , .		1
148	A power scalable 6-bit 1.2GS/s flash ADC with power on/off Track-and-Hold and preamplifier. , 2008, , .		8
149	A power-efficient capacitor structure for high-speed charge recycling SAR ADCs. , 2008, , .		7
150	A pseudo-differential comparator-based pipelined ADC with common mode feedforward technique. , 2008, , .		1
151	Generalized Circuit Techniques for Low-Voltage High-Speed Reset- and Switched-Opamps. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2188-2201.	5.4	5
152	Linearity analysis on a series-split capacitor array for high-speed SAR ADCs. , 2008, , .		6
153	A self-timing switch-driving register by precharge-evaluate logic for high-speed SAR ADCs. , 2008, , .		5
154	A process- and temperature- insensitive current-controlled delay generator for sampled-data systems. , 2008, , .		1
155	Statistical Spectra and Distortion Analysis of Time-Interleaved Sampling Bandwidth Mismatch. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 648-652.	3.0	24
156	Exact Spectra Analysis of Sampled Signals With Jitter-Induced Nonuniformly Holding Effects. IEEE Transactions on Instrumentation and Measurement, 2004, 53, 1279-1288.	4.7	17
157	Timing-mismatch analysis in high-speed analog front-end with nonuniformly holding output. , 0, , .		2
158	Spectra analysis of nonuniformly holding signals for time-interleaved systems with timing mismatches. , 0, , .		1
159	Quantitative noise analysis of jitter-induced nonuniformly sampled-and-held signals. , 0, , .		0
160	A generalized timing-skew-free, multi-phase clock generation platform for parallel sampled-data systems. , 0, , .		1
161	A Novel Low-Voltage Cross-Coupled Passive Sampling Branch for Reset- and Switched-Opamp Circuits. , 0, , .		5
162	A Novel Very Low-Voltage SC-CMFB Technique for Fully-Differential Reset-Opamp Circuits. , 0, , .		2

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163	Novel low-voltage circuit techniques for fully-differential reset- and switched-opamps. , 0, , .		0
164	A power-efficient 1.056 GS/s resolution-switchable 5-bit/6-bit flash ADC for UWB applications. , 0, , .		8