Jean-Luc Gaudiot

List of Publications by Year
in descending order

92 papers	1,042 citations	567144 15 h-index	477173 29 g-index
94 all docs	94 docs citations	94 times ranked	763 citing authors

#	Article	IF	Citations
1	A Novel Spatial-Temporal Multi-Scale Alignment Graph Neural Network Security Model for Vehicles Prediction. IEEE Transactions on Intelligent Transportation Systems, 2023, 24, 904-914.	4.7	43
2	Rise of the Autonomous Machines. Computer, 2022, 55, 64-73.	1.2	4
3	A novel data representation framework based on nonnegative manifold regularisation. Connection Science, 2021, 33, 136-152.	1.8	13
4	Genetic scheduling policy on codelet model. Concurrency Computation Practice and Experience, 2021, 33, 1-1.	1.4	0
5	Engineering Education in the Age of Autonomous Machines. Computer, 2021, 54, 66-69.	1.2	4
6	Π-RT: A Runtime Framework to Enable Energy-Efficient Real-Time Robotic Vision Applications on Heterogeneous Architectures. Computer, 2021, 54, 14-25.	1.2	6
7	<mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" id="d1e326" altimg="si6.svg"><mml:mi>Ï€</mml:mi></mml:math>-Hub: Large-scale video learning, storage, and retrieval on heterogeneous hardware platforms. Future Generation Computer Systems, 2020, 102, 514-523.	4.9	3
8	Computer Education in the Age of COVID-19. Computer, 2020, 53, 114-118.	1.2	15
9	Creating Autonomous Vehicle Systems, Second Edition. Synthesis Lectures on Computer Science, 2020, 8, i-216.	0.3	12
10	Challenges in Detecting an "Evasive Spectre." IEEE Computer Architecture Letters, 2020, 19, 18-21.	1.0	12
11	Autonomous vehicles lite self-driving technologies should start small, go slow. IEEE Spectrum, 2020, 57, 36-49.	0.5	32
12	A Container Based Edge Offloading Framework for Autonomous Driving. IEEE Access, 2020, 8, 33713-33726.	2.6	28
13	Secure Data Storage and Recovery in Industrial Blockchain Network Environments. IEEE Transactions on Industrial Informatics, 2020, 16, 6543-6552.	7.2	179
14	Autonomous Last-Mile Delivery Vehicles in Complex Traffic Environments. Computer, 2020, 53, 26-35.	1.2	18
15	Detecting Malicious Attacks Exploiting Hardware Vulnerabilities Using Performance Counters. , 2019, , .		19
16	Online Detection of Spectre Attacks Using Microarchitectural Traces from Performance Counters. , 2018, , .		20
17	PETRAS. , 2017, , .		4
18	2017: The New Computer Society. Computer, 2017, 50, 5-7.	1.2	0

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19	An effective pre-store/pre-load method exploiting intra-request idle time of NAND flash-based storage devices. Microprocessors and Microsystems, 2017, 50, 222-236.	1.8	1
20	Creating Autonomous Vehicle Systems. Synthesis Lectures on Computer Science, 2017, 6, i-186.	0.3	64
21	Computer Architectures for Autonomous Driving. Computer, 2017, 50, 18-25.	1.2	125
22	A Unified Cloud Platform for Autonomous Driving. Computer, 2017, 50, 42-49.	1.2	49
23	Embracing Changes. Computer, 2017, 50, 4-6.	1.2	0
24	Engineering the New Boundaries of AI. Computer, 2016, 49, 77-79.	1.2	0
25	PETS: Performance, energy and thermal aware scheduler for job mapping with resource allocation in heterogeneous systems. , 2016, , .		5
26	Extending Amdahlâ€™s Law for Heterogeneous Multicore Processor with Consideration of the Overhead of Data Preparation. IEEE Embedded Systems Letters, 2016, 8, 26-29.	1.3	12
27	How can Garbage Collection be energy efficient by dynamic offloading?. , 2015, , .		0
28	Guest Editorial: SBAC-PAD 2013. International Journal of Parallel Programming, 2015, 43, 961-964.	1.1	0
29	Performance-energy efficiency model of heterogeneous parallel multicore system. , 2015, , .		0
30	Network Variation and Fault Tolerant Performance Acceleration in Mobile Devices with Simultaneous Remote Execution. IEEE Transactions on Computers, 2015, 64, 2862-2874.	2.4	1
31	A Performance-Energy Model to Evaluate Single Thread Execution Acceleration. IEEE Computer Architecture Letters, 2015, 14, 99-102.	1.0	4
32	Design of configurable I/O pin control block for improving reusability in multimedia SoC platforms. Multimedia Tools and Applications, 2015, 74, 9055-9066.	2.6	3
33	How many cores do we need to run a parallel workload: A test drive of the Intel SCC platform?. Journal of Parallel and Distributed Computing, 2014, 74, 2582-2595.	2.7	3
34	Boosting CUDA Applications with CPUâ€"GPU Hybrid Computing. International Journal of Parallel Programming, 2014, 42, 384-404.	1.1	23
35	Complexity-Effective Contention Management with Dynamic Backoff for Transactional Memory Systems. IEEE Transactions on Computers, 2014, 63, 1696-1708.	2.4	0
36	Accelerating MapReduce framework on multi-GPU systems. Cluster Computing, 2014, 17, 293-301.	3.5	15

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37	Parallel Sparse Approximate Inverse Preconditioning on Graphic Processing Units. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 1852-1862.	4.0	26
38	Mark-Sharing: A Parallel Garbage Collection Algorithm for Low Synchronization Overhead. , 2013, , .		0
39	Pinned OS/Services: A Case Study of XML Parsing on Intel SCC. Journal of Computer Science and Technology, 2013, 28, 3-13.	0.9	11
40	Practical models for energy-efficient prefetching in mobile embedded systems. Microprocessors and Microsystems, 2013, 37, 1173-1182.	1.8	1
41	Enhancement for Potential Target in Cryptography Algorithms by Applying Processor-in-Memory Architecture. , 2013, , .		0
42	INTRODUCING THE EXTREMELY HETEROGENEOUS ARCHITECTURE. Journal of Interconnection Networks, 2012, 13, 1250010.	0.6	0
43	Minimizing the runtime partial reconfiguration overheads in reconfigurable systems. Journal of Supercomputing, 2012, 61, 894-911.	2.4	14
44	Cooperative heterogeneous computing for parallel processing on CPU/GPU hybrids. , 2012, , .		12
45	Synchronization-Aware Energy Management for VFI-Based Multicore Real-Time Systems. IEEE Transactions on Computers, 2012, 61, 1682-1696.	2.4	42
46	Achieving middleware execution efficiency: hardware-assisted garbage collection operations. Journal of Supercomputing, 2012, 59, 1101-1119.	2.4	21
47	Keynote talk by Dr. Jean-Luc Gaudiot: Fighting Amdahl's law in many-core and GPU parallel architectures with value prediction. , 2011, , .		0
48	Prefetching in Embedded Mobile Systems Can Be Energy-Efficient. IEEE Computer Architecture Letters, 2011, 10, 8-11.	1.0	25
49	RHE: A JVM Courseware. IEEE Transactions on Education, 2011, 54, 141-148.	2.0	9
50	Space-and-Time Efficient Parallel Garbage Collector for Data-Intensive Applications. International Journal of Parallel Programming, 2011, 39, 451-472.	1.1	3
51	Value Prediction and Speculative Execution on GPU. International Journal of Parallel Programming, 2011, 39, 533-552.	1.1	15
52	Workload characterization of cryptography algorithms for hardware acceleration (abstracts only). Performance Evaluation Review, 2011, 39, 20-20.	0.4	0
53	Tolerating Radiation-Induced Transient Faults in Modern Processors. International Journal of Parallel Programming, 2010, 38, 85-116.	1.1	7
54	Network Applications on Simultaneous Multithreading Processors. IEEE Transactions on Computers, 2010, 59, 1200-1209.	2.4	6

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55	The Performance Analysis and Hardware Acceleration of Crypto-computations for Enhanced Security. , 2010, , .		0
56	Hardware-assisted security mechanism: The acceleration of cryptographic operations with low hardware cost. , 2010, , .		6
57	Introducing the New Editor-in-Chief of IEEE Computer Architecture Letters. IEEE Computer Architecture Letters, 2009, 8, 37-38.	1.0	0
58	Special issue of Supercomputing Journal on secure, manageable and controllable grid services. Journal of Supercomputing, 2009, 49, 1-3.	2.4	0
59	A complexity-effective microprocessor design with decoupled dispatch queues and prefetching. Parallel Computing, 2009, 35, 255-268.	1.3	1
60	Potential Impact of Value Prediction on Communication in Many-Core Architectures. IEEE Transactions on Computers, 2009, 58, 759-769.	2.4	20
61	The Impact of Speculative Execution on SMT Processors. International Journal of Parallel Programming, 2008, 36, 361-385.	1.1	6
62	Design and Implementation of an Agent Home Scheme Strategy for Prefetch-Based DSM Systems. International Journal of Parallel Programming, 2008, 36, 521-542.	1.1	0
63	Automatic object and image alignment using Fourier Descriptors. Image and Vision Computing, 2008, 26, 1196-1206.	2.7	19
64	A low-complexity microprocessor design with speculative pre-execution. Journal of Systems Architecture, 2008, 54, 1101-1112.	2.5	0
65	An Efficient Data-Distribution Mechanism in a Processor-In-Memory (PIM) Architecture Applied to Motion Estimation. IEEE Transactions on Computers, 2008, 57, 375-388.	2.4	7
66	The potential of fine-grained value prediction in enhancing the performance of modern parallel machines. , 2008, , .		2
67	Resource sharing control in Simultaneous MultiThreading microarchitectures. , 2008, , .		1
68	Architectural Support for Network Applications on Simultaneous MultiThreading Processors. , 2007, , .		0
69	Features of Future Network Processor Architectures. , 2006, , .		5
70	Speculative pre-execution assisted by compiler (SPEAR). Journal of Parallel and Distributed Computing, 2006, 66, 1076-1089.	2.7	1
71	Adaptive dynamic thread scheduling for simultaneous multithreaded architectures with a detector thread. Journal of Parallel and Distributed Computing, 2006, 66, 1304-1321.	2.7	5
72	Design and evaluation of a hierarchical decoupled architecture. Journal of Supercomputing, 2006, 38, 237-259.	2.4	11

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73	A MULTITHREADED SQL SERVICE. Parallel Processing Letters, 2006, 16, 245-259.	0.4	0
74	Automatic Array Partitioning Based on the Smith Normal Form. International Journal of Parallel Programming, 2005, 33, 35-56.	1.1	0
75	Message from the Guest Editors. International Journal of Parallel Programming, 2005, 33, 451-452.	1.1	0
76	THE NEED FOR ADAPTIVE DYNAMIC THREAD SCHEDULING IN SIMULTANEOUS MULTITHREADING. Parallel Processing Letters, 2004, 14, 327-335.	0.4	2
77	Alias Analysis in Java with Reference-Set Representation for High-Performance Computing. International Journal of Parallel Programming, 2004, 32, 39-76.	1.1	2
78	Non-Strict Execution in Parallel and Distributed Computing. International Journal of Parallel Programming, 2003, 31, 77-105.	1.1	3
79	On a scheme for parallel sorting on heterogeneous clusters. Future Generation Computer Systems, 2002, 18, 353-372.	4.9	5
80	Enhancing Functional and Irregular Parallelism: Stateful Functions and their Semantics. International Journal of Parallel Programming, 2001, 29, 433-460.	1.1	1
81	Exploiting Locality in Single Assignment Data Structures Updated Through Split-Phase Transactions. Cluster Computing, 2001, 4, 281-293.	3.5	2
82	BENCHMARKING CLUSTERS OF WORKSTATIONS THROUGH PARALLEL SORTING AND BSP LIBRARIES. Parallel Processing Letters, 2001, 11, 25-40.	0.4	1
83	An efficient heuristic for code partitioning. Parallel Computing, 2000, 26, 399-426.	1.3	7
84	Analysis of a Heuristic for Code Partitioning. Journal of Supercomputing, 1998, 12, 191-226.	2.4	0
85	Exploiting locality and tolerating remote memory access latency using thread migration. International Journal of Parallel Programming, 1997, 25, 281-304.	1.1	3
86	Data and Workload Distribution in a Multithreaded Architecture. Journal of Parallel and Distributed Computing, 1997, 40, 256-264.	2.7	10
87	Part I: Special Issue on Parallel Architectures and Compilation Techniques. International Journal of Parallel Programming, 1996, 24, 207-208.	1.1	0
88	Parallel Computing with the Sisal Applicative Language: Programmability and Performance Issues. Software - Practice and Experience, 1996, 26, 1025-1051.	2.5	1
89	Incorporating input/output operations into dynamic data-flow graphs. Parallel Computing, 1995, 21, 1285-1311.	1.3	0
90	Learning legal moves in planning problems: A connectionist approach to examining legal moves in the tower-of-hanoi. Engineering Applications of Artificial Intelligence, 1992, 5, 239-245.	4.3	3

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91	Special issue on data-flow computing Guest editors' introduction. Journal of Parallel and Distributed Computing, 1990, 10, 277-278.	2.7	0
92	Occamflow: A methodology for programming multiprocessor systems. Journal of Parallel and Distributed Computing, 1989, 7, 96-124.	2.7	8