Chenyun Pan

List of Publications by Year
in descending order

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51 papers	427 citations	840776 11 h-index	794594 19 g-index
51 all docs	51 docs citations	51 times ranked	490 citing authors

#	Article	IF	Citations
1	Deep Pipeline Circuit for Low-Power Spintronic Devices. IEEE Transactions on Electron Devices, 2021, 68, 1962-1968.	3.0	1
2	Interconnect Technology/System Co-Optimization for Low-Power VLSI Applications Using Ballistic Materials. IEEE Transactions on Electron Devices, 2021, 68, 3513-3519.	3.0	1
3	Memristor-Based Analog Recursive Computation Circuit for Linear Programming Optimization. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 53-61.	1.5	0
4	Fast Linear Programming Optimization Using Crossbar-Based Analog Accelerator. , 2020, , .		0
5	Benchmarking and Optimization of Spintronic Memory Arrays. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 9-17.	1.5	15
6	Accurate Determination of Interlayer Resistivity of 2-D Layered Systems: Graphene Case Study. IEEE Transactions on Electron Devices, 2020, 67, 627-632.	3.0	2
7	A Mixed Signal Architecture for Convolutional Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-26.	2.3	16
8	Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 85-93.	1.5	5
9	Performance Analysis and Enhancement of Negative Capacitance Logic Devices Based on Internally Resistive Ferroelectrics. IEEE Electron Device Letters, 2018, 39, 765-768.	3.9	11
10	Correction to â€œA Nonvolatile Fast-Read Two-Transistor SRAM Based on Spintronic Devicesâ€•[Dec 17 93-100]. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2018, 4, 50-50.	1.5	0
11	Complementary Logic Implementation for Antiferromagnet Field-Effect Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2018, 4, 69-75.	1.5	9
12	Generic system-level modeling and optimization for beyond CMOS device applications. , 2018, , .		0
13	Transient Performance Analysis and Optimization of Crossbar Memory Arrays Using NbO2-Based Threshold Switching Selectors. IEEE Transactions on Electron Devices, 2018, 65, 3214-3220.	3.0	2
14	Modeling Interconnect Variability at Advanced Technology Nodes and Potential Solutions. IEEE Transactions on Electron Devices, 2017, 64, 1246-1253.	3.0	9
15	Nonvolatile Spintronic Memory Array Performance Benchmarking Based on Three-Terminal Memory Cell. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 10-17.	1.5	16
16	Corrections to â€œInterconnect Design and Benchmarking for Charge-Based Beyond-CMOS Device Proposalsâ€•[Apr 16 508-511]. IEEE Electron Device Letters, 2017, 38, 690-690.	3.9	0
17	Beyond-CMOS non-Boolean logic benchmarking: Insights and future directions. , 2017, , .		8
18	An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 101-110.	1.5	35

#	Article	IF	Citations
19	A Nonvolatile Fast-Read Two-Transistor SRAM Based on Spintronic Devices. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2017, 3, 93-100.	1.5	7
20	Performace modeling and optimization for on-chip interconnects in memory arrays. , 2016, , .		0
21	Performance modeling and optimization for on-chip interconnects in cross-bar ReRAM memory arrays. , 2016, , .		0
22	Impact of spintronics transducers on the performance of spin wave logic circuit. , 2016, , .		5
23	Non-Boolean Computing Benchmarking for Beyond-CMOS Devices Based on Cellular Neural Network. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2016, 2, 36-43.	1.5	30
24	Performance analyses and benchmarking for spintronic devices and interconnects. , 2016, , .		2
25	Performance modeling and optimization for on-chip interconnects in STT-MRAM memory arrays. , 2016, , .		1
26	A Proposal for Energy-Efficient Cellular Neural Network Based on Spintronic Devices. IEEE Nanotechnology Magazine, 2016, 15, 820-827.	2.0	34
27	Ultra-High Mobility in Dielectrically Pinned CVD Graphene. IEEE Journal of the Electron Devices Society, 2016, 4, 466-472.	2.1	5
28	Spin-based interconnect technology and design. , 2016, , .		0
29	Interconnect design for conventional and emerging charge-based devices. , 2016, , .		0
30	Performance modeling and optimization for on-chip interconnects in 3D memory arrays. , 2016, , .		0
31	Device/system performance modeling of stacked lateral NWFET logic. , 2016, , .		0
32	Impact of interconnect variability on circuit performance in advanced technology nodes. , 2016, , .		8
33	Interconnect Design and Benchmarking for Charge-Based Beyond-CMOS Device Proposals. IEEE Electron Device Letters, 2016, 37, 508-511.	3.9	11
34	Performace modeling and optimization for on-chip interconnects in memory arrays. , 2015, , .		0
35	Adapting Interconnect Technology to Multigate Transistors for Optimum Performance. IEEE Transactions on Electron Devices, 2015, 62, 3938-3944.	3.0	22
36	System-Level Variation Analysis for Interconnection Networks at Sub-10-nm Technology Nodes Using Multiple Patterning Techniques. IEEE Transactions on Electron Devices, 2015, 62, 2071-2077.	3.0	9

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37	A Paradigm Shift in Local Interconnect Technology Design in the Era of Nanoscale Multigate and Gate-All-Around Devices. IEEE Electron Device Letters, 2015, 36, 274-276.	3.9	24
38	Technology/circuit co-optimization and benchmarking for graphene interconnects at Sub-10nm technology node. , 2015, , .		0
39	Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 1530-1536.	3.0	18
40	A Fast System-Level Design Methodology for Heterogeneous Multi-Core Processors Using Emerging Technologies. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 75-87.	3.6	5
41	Technology/System Codesign and Benchmarking for Lateral and Vertical GAA Nanowire FETs at 5-nm Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 3125-3132.	3.0	36
42	System-level chip/package co-design for multi-core processors implemented with power-gating technique. , 2014, , .		0
43	System-level variation analysis for interconnection networks. , 2014, , .		2
44	A Proposal for a Novel Hybrid Interconnect Technology for the End of Roadmap. IEEE Electron Device Letters, 2014, 35, 250-252.	3.9	41
45	An analytical approach to system-level variation analysis and optimization for multi-core processor. , 2014, , .		1
46	BEOL Scaling Limits and Next Generation Technology Prospects. , 2014, , .		11
47	System-level analysis for 3D interconnection networks. , 2013, , .		5
48	System-level optimization and benchmarking for InAs nanowire based gate-all-around tunneling FETs. , 2013, , .		1
49	System-level performance optimization and benchmarking for on-chip graphene interconnects. , 2012, , .		5
50	System-level optimization and benchmarking of graphene PN junction logic system based on empirical CPI model. , 2012, , .		6
51	Device- and system-level performance modeling for graphene P-N junction logic. , 2012, , .		8