Peng Liu

List of Publications by Year
in descending order

29	178	1307366 7	1125617 13
papers	citations	h-index	g-index

29	29	29	113
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	On a Consistency Testing Model and Strategy for Revealing RISC Processorâ€™s Dark Instructions and Vulnerabilities. IEEE Transactions on Computers, 2022, 71, 1586-1597.	2.4	2
2	IMSC: Instruction set architecture monitor and secure cache for protecting processor systems from undocumented instructions. IET Information Security, 2022, 16, 314-319.	1.1	2
3	A Deep Learning-Based FPGA Function Block Detection Method With Bitstream to Image Transformation. IEEE Access, 2021, 9, 99794-99804.	2.6	3
4	High-Performance Password Recovery Hardware going from GPU to Hybrid CPU-FPGA Platform. IEEE Consumer Electronics Magazine, 2020, , 1-1.	2.3	1
5	Energy-Efficient RAR3 Password Recovery with Dual-Granularity Data Path Strategy. , 2019, , .		4
6	An Energy-Efficient Accelerator Based on Hybrid CPU-FPGA Devices for Password Recovery. IEEE Transactions on Computers, 2019, 68, 170-181.	2.4	20
7	Hadoop Configuration Tuning With Ensemble Modeling and Metaheuristic Optimization. IEEE Access, 2018, 6, 44161-44174.	2.6	20
8	Adaptive Coherence Granularity for Multi-Socket Systems. IEEE Transactions on Computers, 2017, 66, 1302-1312.	2.4	2
9	An Adaptive PAM-4 Analog Equalizer With Boosting-State Detection in the Time Domain. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2907-2916.	2.1	3
10	Half baudâ€rate, low BER PAMâ€4 CDR based on SSâ€MMSE algorithm. Electronics Letters, 2016, 52, 2036-2038.	0.5	2
11	Thread-Aware Adaptive Prefetcher on Multicore Systems. Transactions on Architecture and Code Optimization, 2016, 13, 1-25.	1.6	6
12	Heterogeneous 3-D circuits: Integrating free-space optics with CMOS. Microelectronics Journal, 2016, 50, 66-75.	1.1	8
13	Threads and Data Mapping: Affinity Analysis for Traffic Reduction. IEEE Computer Architecture Letters, 2016, 15, 133-136.	1.0	0
14	Building Expressive and Area-Efficient Directories with Hybrid Representation and Adaptive Multi-Granular Tracking. IEEE Transactions on Computers, 2016, 65, 847-859.	2.4	0
15	Transistorâ€“resistorâ€stacked voltageâ€mode PAMâ€4 symbol generator with improved linearity. Electronics Letters, 2015, 51, 1982-1984.	0.5	0
16	Transitionâ€aware feedâ€forward equaliser for reducing patternâ€dependent jitter in fourâ€level pulseâ€amplitude modulation transmitters. Electronics Letters, 2015, 51, 1263-1265.	0.5	0
17	A Thread-Aware Adaptive Data Prefetcher. , 2014, , .		3
18	DEAM: Decoupled, Expressive, Area-Efficient Metadata Cache. Journal of Computer Science and Technology, 2014, 29, 679-691.	0.9	1

#	Article	IF	Citations
19	Avoiding requestâ€“request type message-dependent deadlocks in networks-on-chips. Parallel Computing, 2013, 39, 408-423.	1.3	1
20	Energy Efficient Run-Time Incremental Mapping for 3-D Networks-on-Chip. Journal of Computer Science and Technology, 2013, 28, 54-71.	0.9	22
21	An efficient protocol with synchronization accelerator for multi-processor embedded systems. Parallel Computing, 2013, 39, 461-474.	1.3	0
22	An efficient scheduler of RTOS for multi/many-core system. Computers and Electrical Engineering, 2012, 38, 785-800.	3.0	7
23	A synergetic operating unit on NoC layer for CMP system. International Journal of High Performance Systems Architecture, 2010, 2, 145.	0.2	1
24	A power-aware mapping approach to map IP cores onto NoCs under bandwidth and latency constraints. Transactions on Architecture and Code Optimization, 2010, 7, 1-30.	1.6	30
25	Building a multi-FPGA-based emulation framework to support networks-on-chip design and verification. International Journal of Electronics, 2010, 97, 1241-1262.	0.9	20
26	An object oriented model scheduling for media-SoC. Journal of Electronics, 2009, 26, 244-251.	0.2	3
27	Optimizing pipeline for a RISC processor with multimedia extension ISA. Journal of Zhejiang University: Science A, 2006, 7, 269-274.	1.3	10
28	32b RISC/DSP media processor: MediaDSP3201. , 2005, , .		4
29	A Hybrid-CPU-FPGA-based Solution to the Recovery of Sha256crypt-hashed Passwords. Iacr Transactions on Cryptographic Hardware and Embedded Systems, 0, , 1-23.	0.0	3