# Pascal Giard

List of Publications by Year
in descending order



| | | | |
|---|---|---|---|
| 33 papers | 885 citations | 1040056 9 h-index | 1281871 11 g-index |
| 34 all docs | 34 docs citations | 34 times ranked | 475 citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Fast Polar Decoders: Algorithm and Implementation. IEEE Journal on Selected Areas in Communications, 2014, 32, 946-957. | 14.0 | 290 |
| 2 | Fast List Decoders for Polar Codes. IEEE Journal on Selected Areas in Communications, 2016, 34, 318-328. | 14.0 | 127 |
| 3 | Flexible and Low-Complexity Encoding and Decoding of Systematic Polar Codes. IEEE Transactions on Communications, 2016, 64, 2732-2745. | 7.8 | 67 |
| 4 | Design of a New Differential Chaos-Shift-Keying System for Continuous Mobility. IEEE Transactions on Communications, 2016, 64, 2066-2078. | 7.8 | 53 |
| 5 | 237ÂGbit/s unrolled hardware polar decoder. Electronics Letters, 2015, 51, 762-763. | 1.0 | 41 |
| 6 | Partitioned successive-cancellation list decoding of polar codes. , 2016, , . | | 36 |
| 7 | PolarBear: A 28-nm FD-SOI ASIC for Decoding of Polar Codes. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2017, 7, 616-629. | 3.6 | 34 |
| 8 | Fast Low-Complexity Decoders for Low-Rate Polar Codes. Journal of Signal Processing Systems, 2018, 90, 675-685. | 2.1 | 33 |
| 9 | Multi-Mode Unrolled Architectures for Polar Decoders. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1443-1453. | 5.4 | 28 |
| 10 | Comparison of Polar Decoders with Existing Low-Density Parity-Check and Turbo Decoders. , 2017, , . | | 28 |
| 11 | Increasing the speed of polar list decoders. , 2014, , . | | 21 |
| 12 | Hardware decoders for polar codes: An overview. , 2016, , . | | 16 |
| 13 | Fast software polar decoders. , 2014, , . | | 14 |
| 14 | A 638 Mbps low-complexity rate 1/2 polar decoder on FPGAs. , 2015, , . | | 13 |
| 15 | Autogenerating software polar decoders. , 2014, , . | | 11 |
| 16 | Low-Latency Software Polar Decoders. Journal of Signal Processing Systems, 2018, 90, 761-775. | 2.1 | 11 |
| 17 | FPGA implementation and evaluation of discrete-time chaotic generators circuits. , 2012, , . | | 10 |
| 18 | On the Tradeoff Between Accuracy and Complexity in Blind Detection of Polar Codes. , 2018, , . | | 10 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Stall pattern avoidance in polynomial product codes. , 2016, , . | | 8 |
| 20 | A multi-Gbps unrolled hardware list decoder for a systematic polar code. , 2016, , . | | 7 |
| 21 | A 9.52 dB NCG FEC Scheme and 162 b/Cycle Low-Complexity Product Decoder Architecture. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1420-1431. | 5.4 | 6 |
| 22 | A Standalone FPGA-Based Miner for Lyra2REv2 Cryptocurrencies. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1194-1206. | 5.4 | 6 |
| 23 | Analog network coding for multi-user spread-spectrum communication systems. , 2014, , . | | 4 |
| 24 | A Lyra2 FPGA Core for Lyra2REv2-Based Cryptocurrencies. , 2019, , . | | 3 |
| 25 | Low-Latency Software Polar Decoders. , 2017, , 31-53. | | 3 |
| 26 | Design of low complexity multiplierless digital filters with optimized free structure using a population-based metaheuristic. , 2011, , . | | 1 |
| 27 | Early Detection for Optimal-Latency Communications in Multi-Hop Links. , 2019, , . | | 1 |
| 28 | An Early-Stopping Mechanism for DSCF Decoding of Polar Codes. , 2020, , . | | 1 |
| 29 | Fast Low-Complexity Hardware Decoders for Low-Rate Polar Codes. , 2017, , 15-30. | | 1 |
| 30 | Unrolled Hardware Architectures for Polar Decoders. , 2017, , 55-71. | | 1 |
| 31 | CORBA communication backplane for design and verification. , 2008, , . | | 0 |
| 32 | Polar Codes. , 2017, , 1-13. | | 0 |
| 33 | Multi-Mode Unrolled Polar Decoding. , 2017, , 73-85. | | 0 |