Hafizur Rahaman

List of Publications by Year
in descending order

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489 papers	3,367 citations	331670 21 h-index	315739 38 g-index
498 all docs	498 docs citations	498 times ranked	1742 citing authors

#	Article	IF	Citations
1	Formation of medium-ring heterocycles by diene and enyne metathesis. Tetrahedron, 2007, 63, 3919-3952.	1.9	188
2	Comparative Performance Analysis of the Dielectrically Modulated Full- Gate and Short-Gate Tunnel FET-Based Biosensors. IEEE Transactions on Electron Devices, 2015, 62, 994-1001.	3.0	151
3	Study and Analysis of the Effects of SiGe Source and Pocket-Doped Channel on Sensing Performance of Dielectrically Modulated Tunnel FET-Based Biosensors. IEEE Transactions on Electron Devices, 2016, 63, 2589-2596.	3.0	141
4	Modeling and Analysis of Crosstalk Induced Effects in Multiwalled Carbon Nanotube Bundle Interconnects: An ABCD Parameter-Based Approach. IEEE Nanotechnology Magazine, 2015, 14, 259-274.	2.0	69
5	Analysis of Crosstalk in Single- and Multiwall Carbon Nanotube Interconnects and Its Impact on Gate Oxide Reliability. IEEE Nanotechnology Magazine, 2011, 10, 1362-1370.	2.0	67
6	Effective fault detection and routing scheme for wireless sensor networks. Computers and Electrical Engineering, 2014, 40, 291-306.	4.8	59
7	To 3D or Not 3D: Choosing a Photogrammetry Workflow for Cultural Heritage Groups. Heritage, 2019, 2, 1835-1851.	1.9	56
8	From photo to 3D to mixed reality: A complete workflow for cultural heritage visualisation and experience. Digital Applications in Archaeology and Cultural Heritage, 2019, 13, e00102.	1.3	49
9	Survey of 3D digital heritage repositories and platforms. Virtual Archaeology Review, 2020, 11, 1.	1.9	45
10	On the Detection of Missing-Gate Faults in Reversible Circuits by a Universal Test Set. , 2008, , .		43
11	Selectivity Tuning of Graphene Oxide Based Reliable Gas Sensor Devices by Tailoring the Oxygen Functional Groups: A DFT Study Based Approach. IEEE Transactions on Device and Materials Reliability, 2017, 17, 738-745.	2.0	43
12	Low Complexity Digit Serial Systolic Montgomery Multipliers for Special Class of ${m GF}(2^{m})$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 847-852.	3.1	42
13	A novel droplet routing algorithm for digital microfluidic biochips. , 2010, , .		36
14	Digital heritage interpretation: a conceptual framework. Digital Creativity, 2018, 29, 208-234.	1.6	35
15	Interpreting Digital Heritage: A Conceptual Model with End-Users' Perspective. International Journal of Architectural Computing, 2011, 9, 99-113.	1.5	32
16	Fault diagnosis in reversible circuits under missing-gate fault model. Computers and Electrical Engineering, 2011, 37, 475-485.	4.8	29
17	Crosstalk and Gate Oxide Reliability Analysis in Graphene Nanoribbon Interconnects. , 2011, , .		28
18	A Post-Synthesis Optimization Technique for Reversible Circuits Exploiting Negative Control Lines. IEEE Transactions on Computers, 2015, 64, 1208-1214.	3.4	28

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19	Stereoselective Synthesis of Tricyclic Pyranoxepin Derivatives by Ruthenium-Catalyzed Enyne Metathesis/Diels-Alder Reaction. Synlett, 2006, 2006, 0466-0468.	1.8	27
20	Tandem Claisen rearrangement and ruthenium catalyzed enyne bond reorganization as a route to the synthesis of tricyclic 1,8-naphthyridinones. Tetrahedron Letters, 2006, 47, 2111-2113.	1.4	26
21	Optimum Test Set for Bridging Fault Detection in Reversible Circuits. , 2007, , .		26
22	3D Digital Heritage Models as Sustainable Scholarly Resources. Sustainability, 2019, 11, 2425.	3.2	24
23	Generator for Test Set Construction of SMGF in Reversible Circuit by Boolean Difference Method. , 2014, , .		22
24	Reduced thickness interconnect model using GNR to avoid crosstalk effects. Journal of Computational Electronics, 2016, 15, 367-380.	2.5	22
25	Load management scheme for energy holes reduction in wireless sensor networks. Computers and Electrical Engineering, 2015, 48, 343-357.	4.8	21
26	Performance analysis of uniaxially strained monolayer black phosphorus and blue phosphorus n-MOSFET and p-MOSFET. Journal of Computational Electronics, 2016, 15, 919-930.	2.5	21
27	Stability Analysis in Top-Contact and Side-Contact Graphene Nanoribbon Interconnects. IETE Journal of Research, 2017, 63, 588-596.	2.6	21
28	A template-based technique for efficient Clifford+T-based quantum circuit implementation. Microelectronics Journal, 2018, 81, 58-68.	2.0	21
29	A Novel Approach for Nearest Neighbor Realization of 2D Quantum Circuits. , 2018, , .		21
30	Exploiting Negative Control Lines in the Optimization of Reversible Circuits. Lecture Notes in Computer Science, 2013, , 209-220.	1.3	20
31	EERIH: Energy efficient routing via information highway in sensor network. , 2011, , .		19
32	Synthesis of Reversible Circuits Using Heuristic Search Method. , 2012, , .		19
33	An Optimized S-Box for Advanced Encryption Standard (AES) Design. , 2012, , .		19
34	Electro-thermal RF modeling and performance analysis of graphene nanoribbon interconnects. Journal of Computational Electronics, 2018, 17, 1695-1708.	2.5	19
35	High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop. , 2018, , .		19
36	Spread Spectrum Image Watermarking with Digital Design. , 2009, , .		18

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37	Derivation of Optimal Test Set for Detection of Multiple Missing-Gate Faults in Reversible Circuits. , 2010, , .		18
38	Modeling and analysis of crosstalk induced overshoot/undershoot effects in multilayer graphene nanoribbon interconnects and its impact on gate oxide reliability. Microelectronics Reliability, 2016, 63, 231-238.	1.7	18
39	A Device Simulation-Based Investigation on Dielectrically Modulated Fringing Field-Effect Transistor for Biosensing Applications. IEEE Sensors Journal, 2017, 17, 1399-1406.	4.7	18
40	Modeling and Analysis of Electro-Thermal Impact of Crosstalk Induced Gate Oxide Reliability in Pristine and Intercalation Doped MLGNR Interconnects. IEEE Transactions on Device and Materials Reliability, 2019, 19, 543-550.	2.0	18
41	EER: Energy Efficient Routing in Wireless Sensor Networks. , 2011, , .		17
42	Reversible logic implementation of AES algorithm. , 2013, , .		16
43	Analysis of a temperature-dependent delay optimization model for GNR interconnects using a wire sizing method. Journal of Computational Electronics, 2018, 17, 1536-1548.	2.5	16
44	Techniques for fault-tolerant decomposition of a multicontrolled Toffoli gate. Physical Review A, 2019, 100, .	2.5	16
45	Investigation on the Effects of Substrate, Back-Gate Bias and Front-Gate Engineering on the Performance of DMTFET-Based Biosensors. IEEE Sensors Journal, 2020, 20, 10405-10414.	4.7	16
46	Investigation of Spark-Gap Discharge in a Regime of Very High Repetition Rate. IEEE Transactions on Plasma Science, 2010, 38, 2752-2757.	1.3	15
47	Optimal Reversible Logic Circuit Synthesis Based on a Hybrid DFS-BFS Technique. , 2010, , .		15
48	Performance modeling and analysis of carbon nanotube bundles for future VLSI circuit applications. Journal of Computational Electronics, 2014, 13, 673-688.	2.5	15
49	On Finding a Defect-free Component in Nanoscale Crossbar Circuits. Procedia Computer Science, 2015, 70, 421-427.	2.0	15
50	Parametric fault detection of analog circuits based on Bhattacharyya measure. Analog Integrated Circuits and Signal Processing, 2017, 93, 477-488.	1.4	15
51	On residue removal in digital microfluidic biochips. , 2011, , .		14
52	Influence of Channel Length and High-K Oxide Thickness on Subthreshold DC Performance of Graded Channel and Gate Stack DG-MOSFETs. Nano, 2016, 11, 1650101.	1.0	14
53	Design of memristor-based up-down counter using material implication logic. , 2016, , .		14
54	FPGA implementation of semi-fragile reversible watermarking by histogram bin shifting in real time. Journal of Real-Time Image Processing, 2018, 14, 193-221.	3.5	14

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55	A Statistical Approach of Analog Circuit Fault Detection Utilizing Kolmogorovâ€“Smirnov Test Method. Circuits, Systems, and Signal Processing, 2021, 40, 2091-2113.	2.0	14
56	Implementing Symmetric Functions with Hierarchical Modules for Stuck-At and Path-Delay Fault Testability. Journal of Electronic Testing: Theory and Applications (JETTA), 2006, 22, 125-142.	1.2	13
57	Notice of Removal: Synthesis of online testable reversible circuit. , 2010, , .		13
58	Crosstalk analysis in Carbon Nanotube interconnects and its impact on gate oxide reliability. , 2010, , .		13
59	Mach-Zehnder Interferometer Based All Optical Reversible Carry-Lookahead Adder. , 2014, , .		13
60	Switching behavior of a double gap pseudospark discharge. IEEE Transactions on Dielectrics and Electrical Insulation, 2015, 22, 3299-3304.	2.9	13
61	Homogeneous droplet routing in DMFB: An enhanced technique for high performance bioassay implementation. The Integration VLSI Journal, 2018, 60, 74-91.	2.1	13
62	Error-Oblivious Sample Preparation With Digital Microfluidic Lab-on-Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 1886-1899.	2.7	13
63	Thermal-Aware Placement of Standard Cells and Gate Arrays: Studies and Observations. , 2008, , .		12
64	Single error correctable bit parallel multipliers over GF(2m). IET Computers and Digital Techniques, 2009, 3, 281.	1.2	12
65	Test Planning in Digital Microfluidic Biochips Using Efficient Eulerization Techniques. Journal of Electronic Testing: Theory and Applications (JETTA), 2011, 27, 657-671.	1.2	12
66	Modeling of IR-Drop induced delay fault in CNT and GNR power distribution networks. , 2012, , .		12
67	Synthesis of circuits based on all-optical Mach-Zehnder Interferometers using Binary Decision Diagrams. Microelectronics Journal, 2018, 71, 19-29.	2.0	12
68	Easily testable realization of GRM and ESOP networks for detecting stuck-at and bridging faults. , 0, , .		11
69	A heuristic method for constructing hexagonal Steiner minimal trees for routing in VLSI. , 0, , .		11
70	Ultra low-power sequential circuit implementation by a Quasi-Static Single phase Adiabatic Dynamic Logic (SPADL). , 2009, , .		11
71	Testable design of ANDâ€“EXOR logic networks with universal test sets. Computers and Electrical Engineering, 2009, 35, 644-658.	4.8	11
72	Unified Digit Serial Systolic Montgomery Multiplication Architecture for Special Classes of Polynomials over GF(2m). , 2010, , .		11

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73	On the design of different concurrent EDC schemes for S-Box and GF(p). , 2010, , .		11
74	Crosstalk overshoot/undershoot analysis and its impact on gate oxide reliability in multi-wall carbon nanotube interconnects. Journal of Computational Electronics, 2011, 10, 360-372.	2.5	11
75	Two-level clustering-based techniques for intelligent droplet routing in digital microfluidic biochips. The Integration VLSI Journal, 2012, 45, 316-330.	2.1	11
76	Nearest-Neighbor and Fault-Tolerant Quantum Circuit Implementation. , 2016, , .		11
77	Parametric Fault Detection in Analog Circuits: A Statistical Approach. , 2016, , .		11
78	Survey on memory management techniques in heterogeneous computing systems. IET Computers and Digital Techniques, 2020, 14, 47-60.	1.2	11
79	The Influence of Collaborative and Multi-Modal Mixed Reality: Cultural Learning in Virtual Heritage. Multimodal Technologies and Interaction, 2021, 5, 79.	2.5	11
80	Accelerated Functional Testing of Digital Microfluidic Biochips. , 2008, , .		10
81	Thermal Aware Placement in 3D ICs. , 2010, , .		10
82	Ant Colony Optimization Based Droplet Routing Technique in Digital Microfluidic Biochip. , 2011, , .		10
83	A new cross contamination aware routing method with intelligent path exploration in digital microfluidic biochips. , 2013, , .		10
84	Implementation of combinational circuits via material implication using memristors. , 2016, , .		10
85	Tuning of electronic properties of edge oxidized armchair graphene nanoribbon by the variation of oxygen amounts and positions. Journal of Materials Science: Materials in Electronics, 2017, 28, 9039-9047.	2.2	10
86	A technique to incorporate both tensile and compressive channel stress in Ge FinFET architecture. Journal of Computational Electronics, 2017, 16, 620-630.	2.5	10
87	Analysis of Crosstalk-Induced Effects in Multilayer Graphene Nanoribbon Interconnects. Journal of Circuits, Systems and Computers, 2017, 26, 1750102.	1.5	10
88	On Designing Testable Reversible Circuits Using Gate Duplication. Communications in Computer and Information Science, 2013, , 322-329.	0.5	10
89	An optoelectronic band-to-band tunnel transistor for near-infrared sensing applications: Device physics, modeling, and simulation. Journal of Applied Physics, 2016, 120, .	2.5	10
90	Multi-source data fusion technique for parametric fault diagnosis in analog circuits. The Integration VLSI Journal, 2022, 84, 92-101.	2.1	10

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91	Scan Chain Design Targeting Dual Power and Delay Optimization for 3D Integrated Circuit. , 2009, , .		9
92	Test Wrapper Design for 3D System-on-Chip Using Optimized Number of TSVs. , 2010, , .		9
93	Modeling of single-wall carbon nanotube interconnects for different process, temperature, and voltage conditions and investigating timing delay. Journal of Computational Electronics, 2012, 11, 349-363.	2.5	9
94	Reversible Logic Circuit Synthesis Using Genetic Algorithm and Particle Swarm Optimization. , 2012, , .		9
95	Performance analysis of multiwalled carbon nanotube bundles. , 2013, , .		9
96	Optimization algorithms for the design of digital microfluidic biochips: A survey. Computers and Electrical Engineering, 2013, 39, 112-121.	4.8	9
97	Derivation of test set for detecting multiple missing-gate faults in reversible circuits. Computers and Electrical Engineering, 2013, 39, 225-236.	4.8	9
98	FPGA and SoC based VLSI architecture of reversible watermarking using rhombus interpolation by difference expansion. , 2014, , .		9
99	An ABCD parameter based modeling and analysis of crosstalk induced effects in Multilayer Graphene Nano Ribbon interconnects. , 2014, , .		9
100	A novel dual purpose spatial domain algorithm for digital image watermarking and cryptography using Extended Hamming Code. , 2015, , .		9
101	BDD-Based Synthesis for All-Optical Mach-Zehnder Interferometer Circuits. , 2015, , .		9
102	An ESOP-Based Reversible Circuit Synthesis Flow Using Simulated Annealing. Advances in Intelligent Systems and Computing, 2015, , 131-144.	0.6	9
103	All optical reversible design of Mach-Zehnder interferometer based Carry-Skip Adder. , 2016, , .		9
104	Impact of gate engineering in enhancement mode n++GaN/InAlN/AlN/GaN HEMTs. Superlattices and Microstructures, 2016, 100, 306-314.	3.1	9
105	Investigating the Applicability of Graphene Nanoribbon as Signal and Power Interconnects for Nanometer Designs. Journal of Circuits, Systems and Computers, 2016, 25, 1650001.	1.5	9
106	Effect of temperature & phonon scattering on the drain current of a MOSFET using SL-MoS2 as its channel material. Superlattices and Microstructures, 2017, 111, 912-921.	3.1	9
107	Analog Circuit Fault Detection by Impulse Response-Based Signature Analysis. Circuits, Systems, and Signal Processing, 2020, 39, 4281-4296.	2.0	9
108	Design of Content Addressable Memory Architecture Using Carbon Nanotube Field Effect Transistors. Lecture Notes in Computer Science, 2012, , 233-242.	1.3	9

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109	Transition count based BIST for detecting multiple stuck-open faults in CMOS circuits. , 0, , .		8
110	Testing of stuck-open faults in generalised Reedâ€“Muller and EXOR sum-of-products CMOS circuits. IEE Proceedings: Computers and Digital Techniques, 2004, 151, 83.	1.6	8
111	UDDN: Unidirectional Data Dissemination via Negotiation. Information Networking, 2008 ICOIN 2008 International Conference on, 2008, , .	0.0	8
112	C-testable bit parallel multipliers over GF (2 m). ACM Transactions on Design Automation of Electronic Systems, 2008, 13, 1-18.	2.6	8
113	Dual Mode VLSI Architecture for Spread Spectrum Image Watermarking using Binary Watermark. Procedia Technology, 2012, 6, 784-791.	1.1	8
114	A Heuristic Method for Co-optimization of Pin Assignment and Droplet Routing in Digital Microfluidic Biochip. , 2012, , .		8
115	Effect of stacking order on device performance of bilayer black phosphorene-field-effect transistor. Journal of Applied Physics, 2015, 118, .	2.5	8
116	Analysis of tunneling currents in multilayer black phosphorous and $$hbox {MoS}_{2}$$ MoS 2 non-volatile flash memory cells. Journal of Computational Electronics, 2016, 15, 129-137.	2.5	8
117	A New FPGA and Programmable SoC Based VLSI Architecture for Histogram Generation of Grayscale Images for Image Processing Applications. Procedia Computer Science, 2016, 93, 139-145.	2.0	8
118	Potentiality of Density-Functional Theory in Analyzing the Devices Containing Graphene-Crystalline Solid Interfaces: A Review. IEEE Transactions on Electron Devices, 2017, 64, 4738-4745.	3.0	8
119	Digital Heritage Interpretation: Learning from the Realm of Real-World. Journal of Interpretation Research, 2017, 22, 53-64.	0.3	8
120	Ab initio study of mono-layer 2-D insulators (X-(OH)2 and h-BN) and their use in MTJ memory device. Microsystem Technologies, 2019, 25, 1909-1917.	2.0	8
121	Prediction and Implementation of Graphene and Other Two-Dimensional Material Based Superconductors: A Review. IEEE Transactions on Applied Superconductivity, 2020, 30, 1-9.	1.7	8
122	DFDNM: A Distributed Fault Detection and Node Management Scheme for Wireless Sensor Network. Communications in Computer and Information Science, 2011, , 68-81.	0.5	8
123	Cost Optimal Design of Nonlinear CA based PRPG for Test Applications. , 2005, , .		7
124	Single Error Correcting Finite Field Multipliers Over GF(2m). , 2008, , .		7
125	On Line Testing of Single Feedback Bridging Fault in Cluster Based FPGA by Using Asynchronous Element. , 2008, , .		7
126	Testing of Digital Microfluidic Biochips Using Improved Eulerization Techniques and the Chinese Postman Problem. , 2010, , .		7

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127	A study on emergency contraceptive practice among nursing staff in Sikkim, India-A cross sectional study. Australasian Medical Journal, 2010, , 667-671.	0.1	7
128	Minimizing Thermal Disparities during Placement in 3D ICs. , 2010, , .		7
129	A novel VLSI architecture for Walsh-Hadamard transform. , 2010, , .		7
130	Modelling, detection and diagnosis of multiple faults in cross referencing DMFBs. , 2012, , .		7
131	System on Biochips: A New Design for Integration of Multiple DMFBs. , 2012, , .		7
132	ESOP-Based Synthesis of Reversible Circuit Using Improved Cube List. , 2013, , .		7
133	Distributed Multipath Fault Tolerance Routing Scheme for Wireless Sensor Networks. , 2013, , .		7
134	An ABCD parameter-based modeling and analysis of crosstalk induced effects in single-walled carbon nanotube bundle interconnects. , 2013, , .		7
135	Faulty TSVs identification and recovery in 3D stacked ICs during pre-bond testing. , 2013, , .		7
136	An ABCD Parameter Based Modeling and Analysis of Crosstalk Induced Effects in Multiwalled Carbon Nanotube Bundle Interconnects. , 2014, , .		7
137	An Improved Reversible Circuit Synthesis Approach using Clustering of ESOP Cubes. ACM Journal on Emerging Technologies in Computing Systems, 2014, 11, 1-16.	2.3	7
138	Session Based Core Test Scheduling for 3D SOCs. , 2014, , .		7
139	Design and implementation of fast FPGA based architecture for reversible watermarking. , 2014, , .		7
140	A Novel Photosensitive Tunneling Transistor for Near-Infrared Sensing Applications: Design, Modeling, and Simulation. IEEE Transactions on Electron Devices, 2015, 62, 1516-1523.	3.0	7
141	Boolean Difference Technique for Detecting All Missing Gate Faults in Reversible Circuits. , 2015, , .		7
142	Improving the Realization of Multiple-Control Toffoli Gates Using the NCVW Quantum Gate Library. , 2016, , .		7
143	All optical design of hybrid adder circuit using terahertz optical asymmetric demultiplexer. , 2018, , .		7
144	Improved Look-Ahead Approaches for Nearest Neighbor Synthesis of 1D Quantum Circuits. , 2019, , .		7

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145	Fast locking, startup-circuit free, low area, 32-phase analog DLL. The Integration VLSI Journal, 2019, 66, 60-66.	2.1	7
146	Improved Cube List Based Cube Pairing Approach for Synthesis of ESOP Based Reversible Logic. Lecture Notes in Computer Science, 2014, , 129-146.	1.3	7
147	Synthesis of symmetric functions using quantum cellular automata. , 2006, , .		6
148	Design of Reversible Finite Field Arithmetic Circuits with Error Detection. , 2008, , .		6
149	Revisiting fidelity. , 2008, , .		6
150	Region Specific Spatial Domain Image Watermnarking Scheme. , 2009, , .		6
151	Method of droplet routing in digital microfluidic biochip. , 2010, , .		6
152	Derivation of Automatic Test Set for Detection of Missing Gate Faults in Reversible Circuits. , 2011, , .		6
153	Simultaneous switching noise and IR drop in graphene nanoribbon power distribution networks. , 2012, , .		6
154	Design of an NoC with on-chip photonic interconnects using adaptive CDMA links. , 2012, , .		6
155	On-Line Error Detection in Digital Microfluidic Biochips. , 2012, , .		6
156	Particle Swarm Optimization Based Circuit Synthesis of Reversible Logic. , 2012, , .		6
157	A design for testability technique for quantum reversible circuits. , 2013, , .		6
158	Optimizing test time for core-based 3-d integrated circuits by a technique of bi-partitioning. , 2014, , .		6
159	RF performance analysis of graphene nanoribbon interconnect. , 2014, , .		6
160	A Cube Pairing Approach for Synthesis of ESOP-Based Reversible Circuit. , 2014, , .		6
161	All Optical Implementation of Mach-Zehnder Interferometer Based Reversible Sequential Counters. , 2015, , .		6
162	Modeling of Crosstalk Induced Effects in Copper-Based Nanointerconnects: An ABCD Parameter Matrix-Based Approach. Journal of Circuits, Systems and Computers, 2015, 24, 1540007.	1.5	6

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163	High-speed decoder design using memristor-based nano-crossbar architecture. , 2016, , .		6
164	Identification of Faulty TSV with a Built-In Self-Test Mechanism. , 2018, , .		6
165	In-memory designing of Delay and Toggle flip-flops utilizing Memristor Aided loGIC (MAGIC). The Integration VLSI Journal, 2019, 66, 24-34.	2.1	6
166	Maximal Defect-Free Component in Nanoscale Crossbar Circuits Amidst Stuck-Open and Stuck-Closed Faults. Journal of Circuits, Systems and Computers, 2019, 28, 1950180.	1.5	6
167	Simulation-Based Power-Loss Optimization of General-Purpose High-Voltage SiC MOSFET Circuit Under High-Frequency Operation. IEEE Access, 2021, 9, 23786-23794.	4.2	6
168	The effect of the stacking arrangement on the device behavior of bilayer MoS2 FETs. Journal of Computational Electronics, 2021, 20, 161-168.	2.5	6
169	Particle Swarm Optimization Based Reversible Circuit Synthesis Using Mixed Control Toffoli Gates. Journal of Low Power Electronics, 2013, 9, 363-372.	0.6	6
170	A new synthesis of symmetric functions. , 0, , .		5
171	C A Based Sensor Node Management Scheme: An Energy Efficient Approach. , 2007, , .		5
172	Analysis, modeling and optimization of transmission gate delay. , 2011, , .		5
173	Group theory based reversible logic synthesis. , 2012, , .		5
174	Unified model for analyzing timing delay and crosstalk effects in Carbon Nanotube interconnects. , 2012, , .		5
175	Implementation of AES Algorithm in UART Module for Secured Data Transfer. , 2012, , .		5
176	Repairing of faulty TSVs using available number of multiplexers in 3D ICs. , 2013, , .		5
177	Builtâ€inâ€selfâ€test technique for diagnosis of delay faults in clusterâ€based field programmable gate arrays. IET Computers and Digital Techniques, 2013, 7, 210-220.	1.2	5
178	Investigating the performance of Short Gate Insulator Less Dielectrically Modulated Tunnel Field Effect Transistor based bio-sensors. , 2015, , .		5
179	Design of content addressable memory cell using carbon nanotube field effect transistors. , 2016, , .		5
180	A new heterogeneous droplet routing technique and its simulator to improve route performance in digital microfluidic biochips. , 2016, , .		5

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181	BDD based synthesis technique for design of high-speed memristor based circuits. , 2016, , .		5
182	A testing scheme for mixed-control based reversible circuits. , 2016, , .		5
183	Analysis of delay fault in GNR power interconnects. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2018, 31, e2308.	1.9	5
184	Design and synthesis of improved reversible circuits using AIGâ€•and MIGâ€based graph data structures. IET Computers and Digital Techniques, 2019, 13, 38-48.	1.2	5
185	Quantum-dot Cellular Automata Latches for Reversible Logic Using Wave Clocking Scheme. IETE Journal of Research, 2023, 69, 309-324.	2.6	5
186	FFMS: Fuzzy Based Fault Management Scheme in Wireless Sensor Networks. Communications in Computer and Information Science, 2012, , 30-38.	0.5	5
187	On the Suitability of Single-Walled Carbon Nanotube Bundle Interconnects for High-Speed and Power-Efficient Applications. Journal of Low Power Electronics, 2014, 10, 479-494.	0.6	5
188	Analysis of temperature dependent power supply voltage drop in graphene nanoribbon and Cu based power interconnects. AIMS Materials Science, 2016, 3, 1493-1506.	1.4	5
189	Mapping symmetric functions to hierarchical modules for path-delay fault testability. , 2003, , .		4
190	Easily Testable Implementation for Bit Parallel Multipliers in GF (2m). , 2006, , .		4
191	Solidâ€State Regioselective Cyclization Initiated by the Electrophilic Attack on the Double Bond by Nâ€Bromosuccinimide on Montmorillonite Kâ€10 Clay Support under Microwave Irradiation. Synthetic Communications, 2007, 37, 1477-1484.	2.1	4
192	Derivation of Reduced Test Vectors for Bit-Parallel Multipliers over GF(2^m). IEEE Transactions on Computers, 2008, 57, 1289-1294.	3.4	4
193	A Galois Field Based Logic Synthesis Approach with Testability. , 2008, , .		4
194	Cell level thermal placement in 3D ICs. , 2010, , .		4
195	Comparative Analysis of Adiabatic Compressor Circuits for Ultra-low Power DSP Application. , 2010, , .		4
196	Optimization of Test Wrapper for TSV Based 3D SOCs. , 2011, , .		4
197	Optimizing Test Wrapper for Embedded Cores Using TSV Based 3D SOCs. , 2011, , .		4
198	Near-optimal Y-routed delay trees in nanometric interconnect design. IET Computers and Digital Techniques, 2011, 5, 36.	1.2	4

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199	A New design of a dual mode bioassay detection analyzer for digital microfluidic biochips. , 2012, , .		4
200	Reversible circuit synthesis using evolutionary algorithm. , 2012, , .		4
201	Voltage controlled current starved delay cell for Positron Emission Tomography specific DLL based high precision TDC implementation. , 2012, , .		4
202	A New Look Ahead Technique for Customized Testing in Digital Microfluidic Biochips. , 2012, , .		4
203	VLSI Architecture for Spread Spectrum Image Watermarking in Walsh-Hadamard Transform Domain Using Binary Watermark. , 2012, , .		4
204	A Cycle Based Reversible Logic Synthesis Approach. , 2013, , .		4
205	Optimal stacking of SOCs in a 3D-SIC for post-bond testing. , 2013, , .		4
206	Digital microfluidic system: A new design for heterogeneous sample based integration of multiple DMFBs. , 2013, , .		4
207	Digital Design and Pipelined Architecture for Reversible Watermarking Based on Difference Expansion Using FPGA. , 2014, , .		4
208	Optimizing DD-based synthesis of reversible circuits using negative control lines. , 2014, , .		4
209	A new algorithm on wavelet based robust invisible digital image watermarking for multimedia security. , 2015, , .		4
210	An adaptive feedback based reversible watermarking algorithm using difference expansion. , 2015, , .		4
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