Vandana Niranjan

List of Publications by Year
in descending order

43	205	1937685 4	1872680 6
papers	citations	h-index	g-index

43	43	43	95
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	COVID-19 Detection using Compressive Sensing. , 2021, , .		0
2	An efficient elite group-based routing protocol for wireless sensor network. International Journal of Electronics, 2020, 107, 1031-1043.	1.4	6
3	Smart Density Based Traffic Light System. , 2020, , .		13
4	Air Quality Management System. , 2020, , .		5
5	Improving the Noise Performance of ROIC Interface Circuit. , 2020, , .		1
6	Noise reduction from grayscale images. , 2020, , .		1
7	Intelligent Clogged Sewer Control System. , 2019, , .		6
8	Intelligent System for Health Monitoring Applications. , 2019, , .		4
9	Efficient FIR Filter Design using Booth Multiplier for VLSI Applications. , 2018, , .		11
10	Frequency Compensation Analysis for Two Stage Amplifier. , 2018, , .		0
11	TurtleBot: Design and Hardware Component Selection. , 2018, , .		12
12	Slew Rate Enhancement. , 2018, , .		4
13	Transconductance boosting of OTA. , 2018, , .		0
14	Improving injection efficiency of gate modulation ROIC interface for HgCdTe IR photodiodes. Microsystem Technologies, 2017, 23, 4073-4080.	2.0	6
15	A new 16-bit high speed and variable stage carry skip adder. , 2017, , .		8
16	Low power filter design using memristor, meminductor and memcapacitor. , 2017, , .		10
17	Active inductor linearization using transistor level techniques. , 2017, , .		0
18	A new 16-bit ALU using variable stage adder and PTL mux. , 2017, , .		3

#	ARTICLE	IF	CITATIONS
19	High gain analog cell using biasing technique via gate and body terminals. , 2017, , .		3
20	Low Power and High Performance Ring Counter Using Pulsed Latch Technique. , 2016, , .		4
21	Performance evaluation of subthreshold Schmitt trigger using body bias techniques. , 2016, , .		9
22	OTA and its application in LPF utilizing the bulk driven technique with various LV-LP topologies. , 2016, , .		5
23	Self-cascode active inductor in 65nm bulk CMOS for low power RF oscillator. , 2015, , .		0
24	Low-voltage gate and body driven self-biased cascode current mirror with enhanced bandwidth. International Journal of Circuits and Architecture Design, 2015, 1, 320.	0.1	4
25	Adiabatic technique for fat tree decoder to be used in flash ADCs. , 2015, , .		1
26	Improving gain bandwidth product using negative resistance and DTMOS technique. , 2015, , .		3
27	A new low voltage highly linear FVFSC current mirror. , 2015, , .		1
28	Performance evaluation of low voltage Schmitt triggers using variable Threshold techniques. , 2015, , .		7
29	PFAL based power efficient mux based decoder. , 2015, , .		4
30	Analog multiplier using DTMOS-CCII suitable for biomedical application. , 2015, , .		5
31	A Novel Technique to Achieve High Bandwidth at Low Supply Voltage. , 2015, , .		3
32	Improving gain of Class-E amplifier using DTMOS for biomedical devices. , 2014, , .		2
33	Bandwidth extension of voltage follower using DTMOS transistor. , 2014, , .		4
34	Bandwidth extension of analog multiplier using dynamic threshold MOS transistor. , 2014, , .		4
35	Low Voltage CMOS Active Inductor with Bandwidth and Linearity Improvement. , 2014, , .		2
36	COMPOSITE TRANSISTOR CELL USING DYNAMIC BODY BIAS FOR HIGH GAIN AND LOW-VOLTAGE APPLICATIONS. Journal of Circuits, Systems and Computers, 2014, 23, 1450108.	1.5	19

#	ARTICLE	IF	CITATIONS
37	Low-voltage and high-speed flipped voltage follower using DTMOS transistor. , 2014, , .		6
38	CMOS active inductor for low voltage and low power wireless applications. , 2013, , .		4
39	Triple well subthreshold CMOS logic using body-bias technique. , 2013, , .		11
40	Low voltage flipped voltage follower based current mirror using DTMOS technique. , 2013, , .		5
41	Subthreshold Logic Using Body-Bias Technique for Digital VLSI Neural Applications. , 2013, , .		0
42	Subthreshold Schmitt trigger using body-bias technique for ultra low power and high performance applications. Russian Microelectronics, 2011, 40, 141-145.	0.5	4
43	Low voltage fourâ€quadrant analog multiplier using dynamic threshold MOS transistors. Microelectronics International, 2009, 26, 47-52.	0.6	5