Sonam Rewari

List of Publications by Year
in descending order

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76 papers	1,522 citations	394421 19 h-index	361022 35 g-index
79 all docs	79 docs citations	79 times ranked	558 citing authors

#	Article	IF	Citations
1	A Dielectric-Modulated Tunnel-FET-Based Biosensor for Label-Free Detection: Analytical Modeling Study and Sensitivity Analysis. IEEE Transactions on Electron Devices, 2012, 59, 2809-2817.	3.0	190
2	An Investigation of Linearity Performance and Intermodulation Distortion of GME CGT MOSFET for RFIC Design. IEEE Transactions on Electron Devices, 2012, 59, 3263-3268.	3.0	137
3	Dielectric Modulated Tunnel Field-Effect Transistorâ€"A Biomolecule Sensor. IEEE Electron Device Letters, 2012, 33, 266-268.	3.9	123
4	Impact of Temperature Variations on the Device and Circuit Performance of Tunnel FET: A Simulation Study. IEEE Nanotechnology Magazine, 2013, 12, 951-957.	2.0	77
5	Numerical modeling of Subthreshold region of junctionless double surrounding gate MOSFET (JLDSG). Superlattices and Microstructures, 2016, 90, 8-19.	3.1	58
6	Gate-All-Around Nanowire MOSFET With Catalytic Metal Gate For Gas Sensing Applications. IEEE Nanotechnology Magazine, 2013, 12, 939-944.	2.0	52
7	Numerical Model of Gate-All-Around MOSFET With Vacuum Gate Dielectric for Biomolecule Detection. IEEE Electron Device Letters, 2012, 33, 1756-1758.	3.9	50
8	Analytical modeling of gate-all-around junctionless transistor based biosensors for detection of neutral biomolecule species. Journal of Computational Electronics, 2018, 17, 288-296.	2.5	50
9	Dielectric Modulated Junctionless Biotube FET (DM-JL-BT-FET) Bio-Sensor. IEEE Sensors Journal, 2021, 21, 16731-16743.	4.7	43
10	Temperature-Dependent Gate-Induced Drain Leakages Assessment of Dual-Metal Nanowire Field-Effect Transistorâ€"Analytical Model. IEEE Transactions on Electron Devices, 2019, 66, 2437-2445.	3.0	41
11	High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for high frequency applications. Microsystem Technologies, 2020, 26, 1697-1705.	2.0	36
12	Improved analog and AC performance with increased noise immunity using nanotube junctionless field effect transistor (NJLFET). Applied Physics A: Materials Science and Processing, 2016, 122, 1.	2.3	34
13	Two-Dimensional Analytical Drain Current Model for Double-Gate MOSFET Incorporating Dielectric Pocket. IEEE Transactions on Electron Devices, 2012, 59, 2567-2574.	3.0	31
14	Hafnium oxide based cylindrical junctionless double surrounding gate (CJLDSG) MOSFET for high speed, high frequency digital and analog applications. Microsystem Technologies, 2019, 25, 1527-1536.	2.0	31
15	Analytical modeling of Junctionless Accumulation Mode Cylindrical Surrounding Gate MOSFET (JAMâ€CSG). International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2016, 29, 1036-1043.	1.9	28
16	Shallow Extension Engineered Dual Material Surrounding Gate (SEE-DM-SG) MOSFET for improved gate leakages, analysis of circuit and noise performance. AEU - International Journal of Electronics and Communications, 2019, 111, 152924.	2.9	28
17	Novel Dual-Metal Junctionless Nanotube Field-Effect Transistors for Improved Analog and Low-Noise Applications. Journal of Electronic Materials, 2021, 50, 108-119.	2.2	28
18	Physics-based analytic modeling and simulation of gate-induced drain leakage and linearity assessment in dual-metal junctionless accumulation nano-tube FET (DM-JAM-TFET). Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	26

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19	Novel design to improve band to band tunneling and gate induced drain leakages (GIDL) in cylindrical gate all around (GAA) MOSFET. Microsystem Technologies, 2019, 25, 1537-1546.	2.0	25
20	Modeling of shallow extension engineered dual metal surrounding gate (SEE-DM-SG) MOSFET gate-induced drain leakage (GIDL). Indian Journal of Physics, 2021, 95, 299-308.	1.8	25
21	Performance investigation of heterogeneous gate dielectric-gate metal engineeredâ€“gate all around-tunnel FET for RF applications. Microsystem Technologies, 2017, 23, 4081-4090.	2.0	23
22	Dual metal Schottky barrier asymmetric gate stack cylindrical gate all around (DM-SB-ASMGS-CGAA) MOSFET for improved analog performance for high frequency application. Microsystem Technologies, 2022, 28, 761-770.	2.0	21
23	Recent Technological Advancement in Surrounding Gate MOSFET for Biosensing Applications - a Synoptic Study. Silicon, 2022, 14, 5133-5143.	3.3	21
24	Charge plasma technique based dopingless accumulation mode junctionless cylindrical surrounding gate MOSFET: analog performance improvement. Applied Physics A: Materials Science and Processing, 2017, 123, 1.	2.3	20
25	Hot-Carrier Reliability of Gate-All-Around MOSFET for RF/Microwave Applications. IEEE Transactions on Device and Materials Reliability, 2013, 13, 245-251.	2.0	19
26	Two Dimensional Analytical Subthreshold Model of Nanoscale Cylindrical Surrounding Gate MOSFET Including Impact of Localised Charges. Journal of Computational and Theoretical Nanoscience, 2012, 9, 602-610.	0.4	18
27	An Accurate Charge-Control-Based Approach for Noise Performance Assessment of a Symmetric Tied-Gate InAlAs/InGaAs DG-HEMT. IEEE Transactions on Electron Devices, 2012, 59, 1644-1652.	3.0	17
28	Gate-Material-Engineered Junctionless Nanowire Transistor (JNT) With Vacuum Gate Dielectric for Enhanced Hot-Carrier Reliability. IEEE Transactions on Device and Materials Reliability, 2016, 16, 360-369.	2.0	16
29	Core-Shell Nanowire Junctionless Accumalation Mode Field-Effect Transistor (CSN-JAM-FET) for High Frequency Applications - Analytical Study. Silicon, 2021, 13, 4371-4379.	3.3	15
30	Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET. IEEE Transactions on Electron Devices, 2017, , 1-8.	3.0	14
31	Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA)for DNA Bio-Molecule Detection. , 2018, , .		13
32	Analytical Modeling of Dielectric Pocket Double-Gate MOSFET Incorporating Hot-Carrier-Induced Interface Charges. IEEE Transactions on Device and Materials Reliability, 2014, 14, 390-399.	2.0	12
33	Polarization dependent charge control model for microwave performance assessment of AlGaN/GaN/AlGaN double heterostructure HEMTs. Journal of Computational Electronics, 2018, 17, 1229-1240.	2.5	12
34	Modeling and simulation of cylindrical surrounding double-gate (CSDG) MOSFET with vacuum gate dielectric for improved hot-carrier reliability and RF performance. Journal of Computational Electronics, 2016, 15, 657-665.	2.5	11
35	Subthreshold Analytical Model of Asymmetric Gate Stack Triple Metal Gate all Around MOSFET (AGSTMGAAFET) for Improved Analog Applications. Silicon, 2022, 14, 4063-4073.	3.3	11
36	Analytical modeling of dual-metal gate stack engineered junctionless accumulation-mode cylindrical surrounding gate (DMGSE-JAM-CSG) MOSFET. Applied Physics A: Materials Science and Processing, 2021, 127, 1.	2.3	10

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37	Impact of doping concentration and donor-layer thickness on the dc characterization of symmetric double-gate and single-gate InAlAs/InGaAs/InP HEMT for nanometer gate dimension-A comparison. , 2010, , .		9
38	Physics-based drain current modeling of gate-all-around junctionless nanowire twin-gate transistor (JN-TGT) for digital applications. Journal of Computational Electronics, 2016, 15, 492-501.	2.5	9
39	Cylindrical gate all around Schottky barrier MOSFET with insulated shallow extensions at source/drain for removal of ambipolarity: a novel approach. Journal of Semiconductors, 2017, 38, 124002.	3.7	9
40	Performance Analysis of Drain Pocket Hetero Gate Dielectric DG-TFET: Solution for Ambipolar Conduction and Enhanced Drive Current. Silicon, 2022, 14, 8097-8107.	3.3	9
41	Modeling and simulation of multi layer gate dielectric double gate tunnel field-effect transistor (DG-TFET). , 2011, , .		8
42	Temperature-Dependent Analytical Model for Microwave and Noise Performance Characterization of $hbox{In}_{0.52}hbox{Al}_{0.48}hbox{As/In}_{m} hbox{Ga}_{1-m}hbox{As}$$(hbox{0.53} leq m leq) Tj ETQq0 2.0 rgBT /Overlock 10		
43	Sheet carrier concentration and currentâ€“voltage analysis of Al0.15Ga0.85N/GaN/Al0.15Ga0.85N double heterostructure hemt incorporating the effect of traps. Microsystem Technologies, 2022, 28, 665-674.	2.0	8
44	SOI Schottky Barrier Nanowire MOSFET with Reduced Ambipolarity and Enhanced Electrostatic Integrity. Journal of Electronic Materials, 2020, 49, 4450-4456.	2.2	7
45	Enhanced Analog Performance and High-Frequency Applications of Dielectric Engineered High-K Schottky Nanowire FET. Silicon, 2022, 14, 9733-9749.	3.3	7
46	Investigation of Electrostatic Integrity of Nanoscale Dual Material Gate Dielectric Pocket Silicon-on-Void (DMGDPSOV) MOSFET for Improved Device Scalability. IEEE Nanotechnology Magazine, 2014, 13, 667-675.	2.0	6
47	Assessment of analog RF performance for insulated shallow extension (ISE) cylindrical surrounding gate (CSG) MOSFET incorporating gate stack. Microsystem Technologies, 2019, 25, 1547-1554.	2.0	6
48	Comparative Study of Silicon-on-Nothing and IIIâ€“V-on-Nothing Architecture for High Speed and Low Power Analog and RF/Digital Applications. IEEE Nanotechnology Magazine, 2013, 12, 978-984.	2.0	5
49	RF characterization of 100â€nm separate gate InAlAs/InGaAs DGâ€HEMT. Microwave and Optical Technology Letters, 2013, 55, 2796-2803.	1.4	5
50	Analysis of Al0.15Ga0.85N/GaN/Al0.15Ga0.85N DH-HEMT for RF and Microwave Frequency Applications. Semiconductors, 2019, 53, 1784-1791.	0.5	5
51	Impact of Temperature and Indium Composition in the Channel on the Microwave Performance of Single-Gate and Double-Gate InAlAs/InGaAs HEMT. IEEE Nanotechnology Magazine, 2013, 12, 965-970.	2.0	4
52	GaN based Dual-Metal Gate Stack Engineered Junctionless-Surrounding-Gate (DMSEJSG) MOSFET for High Power Applications. , 2019, , .		4
53	Extraction of admittance parameters of symmetrically doped AlGaN/GaN/AlGaN DH-HEMT for microwave frequency applications. Microsystem Technologies, 2021, 27, 4065-4072.	2.0	4
54	<scp>SiC</scp>â€based analytical model for gateâ€stack dual metal nanowire<scp>FET</scp>with enhanced analog performance. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2022, 35, .	1.9	4

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55	Quantum modeling of electron confinement in double triangular quantum well formed in nanoscale symmetric double-gate InAlAs/InGaAs/InP HEMT. , 2011, , .		3
56	Temperature dependent model for Dielectric Pocket Double Gate (DPDG) MOSFET: A novel device architecture. , 2012, , .		3
57	Analytical model for a dielectric modulated double gate FET (DM-DG-FET) biosensor. , 2012, , .		3
58	Intrinsic admittance parameter for separate gate InA1As/InGaAs DG-HEMT for 100 nm gate length. , 2013, , .		3
59	GaN based Junctionless Double Surrounding Gate (JLDSG) MOSFET for high power, high voltage and high frequency applications. , 2016, , .		3
60	Oxide Stack Engineered Double Surrounding Gate (OSE-DSG) MOSFET for Submillimeter Analog Application. , 2018, , .		3
61	Traps induced Greens function based mathematical modeling for BaTiO3â€“SrTiO3 gate stack dual metal GAA MOSFET. Semiconductor Science and Technology, 2019, 34, 115002.	2.0	3
62	Junctionless Accumulation Mode Ferroelectric FET (JAM-FE-FET) for High Frequency Digital and Analog Applications. Silicon, 2022, 14, 7245-7255.	3.3	3
63	Asymmetric gate oxide Tunnel Field Effect Transistor for improved circuit performance. , 2012, , .		2
64	RF performance analysis and small signal parameter extraction of Cylindrical Surrounding Double Gate MOSFETs for sub-millimeter wave applications. , 2014, , .		2
65	CSDG MOSFET: An Advanced novel architecture for CMOS technology. , 2015, , .		2
66	Linearity and Intermodulation Distortion Assessment of Underlap Engineered Cylindrical Junctionless Surrounding Gate MOSFET for Low Noise CMOS RFIC Design. , 2019, , .		2
67	Gate - Stack Dual Metal (DM) Nanowire FET with Enhanced Analog Performance for High Frequency Applications. , 2021, , .		2
68	Temperature dependency and linearity assessment of dual-metal gate stack junctionless accumulation-mode cylindrical surrounding gate (DMGS-JAM-CSG) MOSFET. Physica Scripta, 2021, 96, 124055.	2.5	2
69	Material engineering in Cylindrical Surrounding Double Gate (CSDG) MOSFETs for enhanced electrostatic integrity and RF performance. , 2014, , .		1
70	Interface trap-dependent linearity assessment in single and dual metal gate junctionless accumulation mode (surrounding gate) nanowire MOSFET. Applied Physics A: Materials Science and Processing, 2019, 125, 1.	2.3	1
71	Performance evaluation of dielectric modulation and metalloid T-shaped source/drain on gate-all-around junctionless transistor for improved analog/RF application. Journal of Materials Science: Materials in Electronics, 2021, 32, 10943-10950.	2.2	1
72	Performance investigation and linearity analysis of new cylindrical MOSFET for wireless applications. , 2015, , .		0

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73	AC analysis of Junctionless Double Surrounding Gate (JLDSG) MOSFET for Tera Hertz applications. , 2016, , .		0
74	RF Performance comparison of Dual Material Gate (DMG) and Conventional AlGaN/GaN High Electron Mobility Transistor. , 2018, , .		0
75	Simulating Optical Behavior of Nano Dimensional InAlAs/InGaAs HEMT for IoT Applications. , 2018, , .		0
76	Insulated Shallow Extension Dual Metal Junctionless Accumulation Mode MOSFET (ISE-DMJAM-MOSFET). , 2021, , .		0