

# Sabyasachee Banerjee

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/1884996/publications.pdf>

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14  
papers

36  
citations

3311381

1  
h-index

2917675

2  
g-index

15  
all docs

15  
docs citations

15  
times ranked

24  
citing authors

#	ARTICLE	IF	CITATIONS
1	A Graph-Based 3D IC Partitioning Technique. , 2014, , .		11
2	Test-Time Reduction for Power-Aware 3D-SoC. , 2018, , .		7
3	Image steganography by closest pixel-pair mapping. , 2014, , .		4
4	A thermal aware 3D IC partitioning technique. , 2014, , .		3
5	Partitioning-based test time reduction for core-based 3DICs. , 2015, , .		2
6	A placement optimization technique for 3D IC. , 2017, , .		2
7	Fast algorithms for test optimization of core based 3D SoC. The Integration VLSI Journal, 2021, 77, 70-88.	2.1	2
8	Power-aware test optimization for core-based 3D-SOCs under TSV-constraints. , 2016, , .		1
9	A Deterministic Multi-layered Partitioning Tool for Wire-Length Reduction of Monolithic 3D-IC. , 2019, , .		1
10	Speed Optimization in an Unplanned Lane Traffic Using Swarm Intelligence and Population Knowledge Base Oriented Performance Analysis. Advances in Intelligent and Soft Computing, 2012, , 471-480.	0.2	1
11	Bio-inspired Computational Optimization of Speed in an Unplanned Traffic and Comparative Analysis Using Population Knowledge Base Factor. Advances in Intelligent and Soft Computing, 2012, , 977-987.	0.2	1
12	Micro-Bump Assignment for Efficient Routing on Re-Distribution Layer (RDL) in 3D-ICs. , 2017, , .		0
13	Designing balanced wrapper chains in 3D SoC under constrained TSVs. Innovations in Systems and Software Engineering, 2021, 17, 219-230.	2.1	0
14	A TSV Constrained Algorithm for Designing Balanced Wrapper Chains in 3D SoC. Lecture Notes in Networks and Systems, 2022, , 35-47.	0.7	0