Farid N Najm

List of Publications by Year
in descending order

33	463	1163117 8	940533 16
papers	citations	h-index	g-index

36	36	36	175
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Experimental Validation of a Novel Methodology for Electromigration Assessment in On-Chip Power Grids. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4837-4850.	2.7	3
2	Novel physics-based tool-prototype for electromigration assessment in commercial-grade power delivery networks. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2021, 39, .	1.2	8
3	Equivalent circuits for electromigration. Microelectronics Reliability, 2021, 123, 114200.	1.7	6
4	Electromigration simulation and design considerations for integrated circuit power grids. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2020, 38, .	1.2	5
5	Electromigration checking using a stochastic effective current model. , 2020, , .		0
6	Power Scheduling With Active <inline-formula> <tex-math notation="LaTeX">RC </tex-math> </inline-formula> Power Grids. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 444-457.	3.1	3
7	Power Grid Electromigration Checking Using Physics-Based Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1317-1330.	2.7	70
8	Electromigration Check: Where the Design and Reliability Methodologies Meet. IEEE Transactions on Device and Materials Reliability, 2018, 18, 498-507.	2.0	19
9	Generating Current Constraints to Guarantee RLC Power Grid Safety. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-39.	2.6	0
10	Parallel Simulation-Based Verification of RC Power Grids. , 2017, , .		2
11	Power scheduling with active power grids. , 2017, , .		1
12	Power grid verification under transient constraints. , 2017, , .		1
13	Fast physics-based electromigration assessment by efficient solution of linear time-invariant (LTI) systems. , 2017, , .		11
14	Fast Vectorless RLC Grid Verification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, , 1-1.	2.7	2
15	Fast physics-based electromigration checking for on-die power grids. , 2016, , .		15
16	Generating voltage drop aware current budgets for RC power grids. , 2016, , .		1
17	Generating Current Budgets to Guarantee Power Grid Safety. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1914-1927.	2.7	4
18	Generating circuit current constraints to guarantee power grid safety. , 2015, , .		4

#	Article	IF	Citations
19	Redundancy-Aware Power Grid Electromigration Checking Under Workload Uncertainties. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1509-1522.	2.7	4
20	Redundancy-aware Electromigration checking for mesh power grids. , 2013, , .		24
21	Overview of vectorless/early power grid verification. , 2012, , .		13
22	Maximum Circuit Activity Estimation Using Pseudo-Boolean Satisfiability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 271-284.	2.7	8
23	Efficient Block-Based Parameterized Timing Analysis Covering All Potentially Critical Paths. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 472-484.	2.7	5
24	Fast Vectorless Power Grid Verification Under an RLC Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 691-703.	2.7	20
25	Verification and Codesign of the Package and Die Power Delivery System Using Wavelets. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 92-102.	2.7	18
26	Low-Power Programmable FPGA Routing Circuitry. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 1048-1060.	3.1	39
27	Full-Chip Model for Leakage-Current Estimation Considering Within-Die Correlation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 874-887.	2.7	3
28	Early Analysis and Budgeting of Margins and Corners Using Two-Sided Analytical Yield Models. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1826-1839.	2.7	1
29	A Linear-Time Approach for Static Timing Analysis Covering All Process Corners. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1291-1304.	2.7	21
30	A Yield Model for Integrated Circuits and its Application to Statistical Timing Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 574-591.	2.7	19
31	Variations-Aware Low-Power Design and Block Clustering With Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 746-757.	3.1	3
32	A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting-Match Scheme. , 2006, , .		52
33	A static pattern-independent technique for power grid voltage integrity verification. , 2003, , .		78