Houman Homayoun

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

57 papers	397 citations	11 h-index	16 g-index
69 ext. papers	619 ext. citations	2.1 avg, IF	4.09 L-index

#	Paper	IF	Citations
57	Security Threats in Cloud Rooted from Machine Learning-Based Resource Provisioning Systems. *Communications in Computer and Information Science*, **2022**, 22-32	0.3	
56	Cloak & Co-locate: Adversarial Railroading of Resource Sharing-based Attacks on the Cloud **2021**,		2
55	Cyclic Sparsely Connected Architectures: From foundations to applications. *IEEE Solid-State Circuits Magazine*, **2021**, 13, 64-76	1.5	
54	A Neural Network-based Cognitive Obfuscation Towards Enhanced Logic Locking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	0
53	Towards Accurate Run-Time Hardware-Assisted Stealthy Malware Detection: A Lightweight, yet Effective Time Series CNN-Based Approach. *Cryptography*, **2021**, 5, 28	1.9	3
52	Data Flow Obfuscation: A New Paradigm for Obfuscating Circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 643-656	2.6	1
51	Deep graph transformation for attributed, directed, and signed networks. *Knowledge and Information Systems*, **2021**, 63, 1305-1337	2.4	2
50	Ontology-Driven Framework for Trend Analysis of Vulnerabilities and Impacts in IoT Hardware **2021** ,		2
49	Imitating Functional Operations for Mitigating Side-Channel Leakage. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
48	From Cryptography to Logic Locking: A Survey on the Architecture Evolution of Secure Scan Chains. *IEEE Access*, **2021**, 9, 73133-73151	3.5	1
47	Automatic Detection of Respiratory Symptoms Using a Low Power Multi-Input CNN Processor. *IEEE Design and Test*, **2021**, 1-1	1.4	5
46	A Hardware Accelerator for Language Guided Reinforcement Learning. *IEEE Design and Test*, **2021**, 1-1	1.4	2
45	AVATAR: NN-Assisted Variation Aware Timing Analysis and Reporting for Hardware Trojan Detection. *IEEE Access*, **2021**, 9, 92881-92900	3.5	1
44	Adaptive Performance Modeling of Data-intensive Workloads for Resource Provisioning in Virtualized Environment. *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*, **2021**, 5, 1-24	0.8	2
43	Cyclic Sparsely Connected Architectures for Compact Deep Convolutional Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-14	2.6	3
42	Enabling Micro AI for Securing Edge Devices at Hardware Level. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2021**, 11, 803-815	5.2	1
41	Energy-Efficient Hardware for Language Guided Reinforcement Learning **2020**,		6

40	Comprehensive Evaluation of Machine Learning Countermeasures for Detecting Microarchitectural Side-Channel Attacks **2020**,		6
39	Hybrid-shield **2020**,		4
38	ICNN. *Transactions on Embedded Computing Systems*, **2020**, 18, 1-27	1.8	3
37	. *IEEE Access*, **2020**, 8, 138508-138528	3.5	4
36	SCARF: Detecting Side-Channel Attacks at Real-time using Low-level Hardware Features **2020**,		11
35	Recent Advancements in Microarchitectural Security: Review of Machine Learning Countermeasures **2020**,		4
34	2SMaRT: A Two-Stage Machine Learning-Based Approach for Run-Time Specialized Hardware-Assisted Malware Detection **2019**,		33
33	On the Complexity Reduction of Dense Layers from O(N2) to O(NlogN) with Cyclic Sparsely Connected Layers **2019**,		10
32	Adversarial Attack on Microarchitectural Events based Malware Detectors **2019**,		19
31	Lightweight Node-level Malware Detection and Network-level Malware Confinement in IoT Networks **2019**,		8
30	Resource-Efficient Wearable Computing for Real-Time Reconfigurable Machine Learning: A Cascading Binary Classification **2019**,		1
29	Sequence-crafter **2019**,		1
28	**2019**,		2
27	Security and Complexity Analysis of LUT-based Obfuscation: From Blueprint to Reality **2019**,		7
26	Power conversion efficiency-aware mapping of multithreaded applications on heterogeneous architectures: A comprehensive parameter tuning **2018**,		5
25	ElasticCore: A Dynamic Heterogeneous Platform With Joint Core and Voltage/Frequency Scaling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 249-261	2.6	2
24	LUT-Lock: A Novel LUT-Based Logic Obfuscation for FPGA-Bitstream and ASIC-Hardware Protection **2018**,		10
23	Compressive Sensing on Storage Data: An Effective Solution to Alleviate I/0 Bottleneck in Data-Intensive Workloads **2018**,		2

22	An Energy-Efficient Programmable Manycore Accelerator for Personalized Biomedical Applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 96-109	2.6	12
21	Special Session: Advances and Throwbacks in Hardware-Assisted Security **2018**,		10
20	Benchmarking the Capabilities and Limitations of SAT Solvers in Defeating Obfuscation Schemes **2018**,		7
19	Energy-aware and Machine Learning-based Resource Provisioning of In-Memory Analytics on Cloud **2018**,		8
18	Ensemble Learning for Effective Run-Time Hardware-Based Malware Detection: A Comprehensive Analysis and Classification **2018**,		30
17	LESS: Big data sketching and Encryption on low power platform **2017**,		4
16	Big vs little core for energy-efficient Hadoop computing **2017**,		4
15	Smart Grid on Chip: Work Load-Balanced On-Chip Power Delivery. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2538-2551	2.6	5
14	MeNa: A memory navigator for modern hardware in a scale-out environment **2017**,		12
13	Analyzing Hardware Based Malware Detectors **2017**,		27
12	Machine Learning-Based Approaches for Energy-Efficiency Prediction and Scheduling in Composite Cores Architectures **2017**,		19
11	Scheduling multithreaded applications onto heterogeneous composite cores architecture **2017**,		2
10	Architecture Exploration for Energy-Efficient Embedded Vision Applications: From General Purpose Processor to Domain Specific Accelerator **2016**,		7
9	Characterizing Hadoop applications on microservers for performance and energy efficiency optimizations **2016**,		9
8	Comparative analysis of hybrid Magnetic Tunnel Junction and CMOS logic circuits **2016**,		2
7	Comparative analysis of robustness of spin transfer torque based look up tables under process variations **2016**,		1
6	Accelerating Big Data Analytics Using FPGAs **2015**,		15
5	Accelerating Machine Learning Kernel in Hadoop Using FPGAs **2015**,		18

List of Publications

4	Realizing complexity-effective on-chip power delivery for many-core platforms by exploiting optimized mapping **2015**,	5
3	Power and performance characterization, analysis and tuning for energy-efficient edge detection on atom and ARM based platforms **2015**,	4
2	Energy-efficient acceleration of big data analytics applications using FPGAs **2015**,	28
1	Enabling dynamic heterogeneity through core-on-core stacking **2014**,	2