Won Woo Ro

List of Publications by Year
in descending order

65 papers	634 citations	1162889 8 h-index	887953 17 g-index
65 all docs	65 docs citations	65 times ranked	460 citing authors

#	Article	IF	Citations
1	A Malicious Pattern Detection Engine for Embedded Security Systems in the Internet of Things. Sensors, 2014, 14, 24188-24211.	2.1	87
2	Warped-compression. , 2015, , .		81
3	Fast CU Depth Decision for HEVC Using Neural Networks. IEEE Transactions on Circuits and Systems for Video Technology, 2019, 29, 1462-1473.	5.6	50
4	Access Pattern-Aware Cache Management for Improving Data Utilization in GPU. , 2017, , .		44
5	Warped-Slicer: Efficient Intra-SM Slicing through Dynamic Resource Partitioning for GPU Multiprogramming. , 2016, , .		42
6	Virtual Thread: Maximizing Thread-Level Parallelism beyond GPU Scheduling Limit. , 2016, , .		33
7	Warped-preexecution: A GPU pre-execution approach for improving latency hiding. , 2016, , .		29
8	Boosting CUDA Applications with CPUâ€“GPU Hybrid Computing. International Journal of Parallel Programming, 2014, 42, 384-404.	1.1	23
9	APRES. Computer Architecture News, 2016, 44, 191-203.	2.5	20
10	Parallel GPU architecture simulation framework exploiting work allocation unit parallelism. , 2013, , .		17
11	Improving Energy Efficiency of GPUs through Data Compression and Compressed Execution. IEEE Transactions on Computers, 2017, 66, 834-847.	2.4	16
12	WIR: Warp Instruction Reuse to Minimize Repeated Computations in GPUs. , 2018, , .		15
13	SPACE: Locality-Aware Processing in Heterogeneous Memory for Personalized Recommendations. , 2021, , .		14
14	Highly Secure Mobile Devices Assisted with Trusted Cloud Computing Environments. ETRI Journal, 2015, 37, 348-358.	1.2	12
15	Duplo: Lifting Redundant Memory Accesses of Deep Neural Networks for GPU Tensor Cores. , 2020, , .		10
16	FineReg: Fine-Grained Register File Management for Augmenting GPU Throughput. , 2018, , .		9
17	Accelerating HEVC transcoder by exploiting decoded quadtree. , 2014, , .		8
18	Hi-End: Hierarchical, Endurance-Aware STT-MRAM-Based Register File for Energy-Efficient GPUs. IEEE Access, 2020, 8, 127768-127780.	2.6	8

#	Article	IF	Citations
19	REACT: Scalable and High-Performance Regular Expression Pattern Matching Accelerator for In-Storage Processing. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 1137-1151.	4.0	8
20	Measuring error-tolerance in SRAM architecture on hardware accelerated neural network. , 2016, , .		7
21	Dynamic Load Balancing of Dispatch Scheduling for Solid State Disks. IEEE Transactions on Computers, 2017, 66, 1034-1047.	2.4	7
22	Hardware implementation of a tessellation accelerator for the OpenVG standard. IEICE Electronics Express, 2010, 7, 440-446.	0.3	6
23	A Low-Cost Standard Mode MPI Hardware Unit for Embedded MPSoC. IEICE Transactions on Information and Systems, 2011, E94-D, 1497-1501.	0.4	6
24	Adaptive Cooperation of Prefetching and Warp Scheduling on GPUs. IEEE Transactions on Computers, 2019, 68, 609-616.	2.4	6
25	Integrity Protection for Big Data Processing with Dynamic Redundancy Computation. , 2015, , .		5
26	Server side, play buffer based quality control for adaptive media streaming. Multimedia Tools and Applications, 2016, 75, 5397-5415.	2.6	5
27	True motion compensation with feature detection for frame rate up-conversion. , 2015, , .		4
28	A Performance-Energy Model to Evaluate Single Thread Execution Acceleration. IEEE Computer Architecture Letters, 2015, 14, 99-102.	1.0	4
29	Parallel GPU Architecture Simulation Framework Exploiting Architectural-Level Parallelism with Timing Error Prediction. IEEE Transactions on Computers, 2016, 65, 1253-1265.	2.4	4
30	Dynamic Resizing on Active Warps Scheduler to Hide Operation Stalls on GPUs. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 3142-3156.	4.0	4
31	WASP: Selective Data Prefetching with Monitoring Runtime Warp Progress on GPUs. IEEE Transactions on Computers, 2018, 67, 1366-1373.	2.4	4
32	PIMCaffe: Functional Evaluation of a Machine Learning Framework for In-Memory Neural Processing Unit. IEEE Access, 2021, 9, 96629-96640.	2.6	4
33	Simultaneous and Speculative Thread Migration for Improving Energy Efficiency of Heterogeneous Core Architectures. IEEE Transactions on Computers, 2018, 67, 498-512.	2.4	4
34	Architectural investigation of matrix data layout on multicore processors. Future Generation Computer Systems, 2014, 37, 64-75.	4.9	3
35	Exploiting Pseudo-Quadtree Structure for Accelerating HEVC Spatial Resolution Downscaling Transcoder. IEEE Transactions on Multimedia, 2018, 20, 2262-2275.	5.2	3
36	Efficient and reliable NAND flash channel for high-speed solid state drives. , 2018, , .		3

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37	Check-In: In-Storage Checkpointing for Key-Value Store System Leveraging Flash-Based SSDs. , 2020, , .		3
38	Access Characteristic-based Cache Replacement Policy in an SSD. , 2020, , .		3
39	CASH-RF: A Compiler-Assisted Hierarchical Register File in GPUs. IEEE Embedded Systems Letters, 2022, 14, 187-190.	1.3	3
40	Workload synthesis: Generating benchmark workloads from statistical execution profile. , 2014, , .		2
41	An accelerated separable median filter with sorting networks. , 2015, , .		2
42	A frequency scaling model for energy efficient DVFS designs based on circuit delay optimization. , 2015, , .		2
43	Exploiting Thread-Level Parallelism on HEVC by Employing a Reference Dependency Graph. IEEE Transactions on Circuits and Systems for Video Technology, 2016, 26, 736-749.	5.6	2
44	Interaction Data Analysis for Personalized Recommendation System. , 2020, , .		2
45	A Novel Sequential Tree Algorithm Based on Scoreboard for MPI Broadcast Communication. IEICE Transactions on Information and Systems, 2011, E94-D, 2523-2527.	0.4	1
46	Hyper threading-aware Virtual Machine migration. , 2014, , .		1
47	Multicore speedup models using frequency scaling with fixed power budget. , 2014, , .		1
48	Development of efficient VCPU pinning mechanism in Xen. , 2014, , .		1
49	Enhancing Software Dependability and Security with Hardware Supported Instruction Address Space Randomization. , 2015, , .		1
50	Contention-Free Fair Queuing for High-Speed Storage with RAID-0 Architecture. , 2015, , .		1
51	Network Variation and Fault Tolerant Performance Acceleration in Mobile Devices with Simultaneous Remote Execution. IEEE Transactions on Computers, 2015, 64, 2862-2874.	2.4	1
52	Another Look at Secure Big Data Processing: Formal Framework and a Potential Approach. , 2015, , .		1
53	OverCome: Coarse-Grained Instruction Commit with Handover Register Renaming. IEEE Transactions on Computers, 2019, 68, 1802-1816.	2.4	1
54	Contents-aware partitioning algorithm for parallel high efficiency video coding. Multimedia Tools and Applications, 2019, 78, 11427-11442.	2.6	1

#	Article	IF	Citations
55	Mark-Sharing: A Parallel Garbage Collection Algorithm for Low Synchronization Overhead. , 2013, , .		0
56	LUT based secure cloud computing — An implementation using FPGAs. , 2014, , .		0
57	DPM: Data Partitioning Method for pipelined MapReduce on GPU. , 2014, , .		0
58	Maximizing DRAM performance using selective operating frequency boosting. , 2014, , .		0
59	Swarm Processor System: hardware process scheduler based energy efficient multi-core system. IEICE Electronics Express, 2014, 11, 20140424-20140424.	0.3	0
60	Accelerating gesture recognition algorithm using coarse grained reconfigurable architectures. , 2014, , .		0
61	Fairness-aware thread scheduling for multithreaded program using IntelÂ® Software Guarded Extensions. , 2016, , .		0
62	Characterizing convolutional neural network workloads on a detailed GPU simulator. , 2017, , .		0
63	BODCA: Heterogeneous CPU-GPU computing system with Bandwidth-Optimized DRAM cache design. , 2020, , .		0
64	Two-Stage In-Storage Processing and Scheduling for Pattern Matching Applications. IEEE Access, 2021, 9, 95702-95715.	2.6	0
65	FLIXR: Embedding Index into Flash Translation Layer in SSDs. IEEE Transactions on Computers, 2022, , 1-1.	2.4	0