

Seong-Jin Oh

List of Publications by Year in descending order

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citing authors

#	ARTICLE	IF	CITATIONS
1	A High-Efficiency Triple-Mode Active Rectifier With Gate Charge Recycling Technique for Wireless Power Transfer System. IEEE Access, 2022, 10, 45943-45953.	4.2	2
2	A 15-W Quadruple-Mode Reconfigurable Bidirectional Wireless Power Transceiver With 95% System Efficiency for Wireless Charging Applications. IEEE Transactions on Power Electronics, 2021, 36, 3814-3827.	7.9	9
3	A Design of Adaptive Control and Communication Protocol for SWIPT System in 180 nm CMOS Process for Sensor Applications. Sensors, 2021, 21, 848.	3.8	2
4	A High-Efficient Wireless Power Receiver for Hybrid Energy-Harvesting Sources. IEEE Transactions on Power Electronics, 2021, 36, 11148-11162.	7.9	19
5	An Ultra-Low-Power 2.4 GHz All-Digital Phase-Locked Loop With Injection-Locked Frequency Multiplier and Continuous Frequency Tracking. IEEE Access, 2021, 9, 152984-152992.	4.2	2
6	A 2.45 GHz High Efficiency CMOS RF Energy Harvester with Adaptive Path Control. Electronics (Switzerland), 2020, 9, 1107.	3.1	9
7	A Low-Power Multichannel Time-to-Digital Converter Using All-Digital Nested Delay-Locked Loops With 50-ps Resolution and High Throughput for LiDAR Sensors. IEEE Transactions on Instrumentation and Measurement, 2020, 69, 9262-9271.	4.7	29
8	A Design of 6.8 mW All Digital Delay Locked Loop With Digitally Controlled Dither Cancellation for TDC in Ranging Sensor. IEEE Access, 2020, 8, 57722-57732.	4.2	5
9	Modeling of SWIPT System with ASK Modulation in LabVIEW. , 2019, , .		1
10	A Fully Integrated Bluetooth Low-Energy Transceiver with Integrated Single Pole Double Throw and Power Management Unit for IoT Sensors. Sensors, 2019, 19, 2420.	3.8	10
11	A 3.9 mW Bluetooth Low-Energy Transmitter Using All-Digital PLL-Based Direct FSK Modulation in 55 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3037-3048.	5.4	17
12	Low power FSK transceiver using ADPLL with direct modulation and integrated SPDT for BLE application. , 2018, , .		1
13	A Triple-Mode Wireless Power-Receiving Unit With 85.5% System Efficiency for A4WP, WPC, and PMA Applications. IEEE Transactions on Power Electronics, 2018, 33, 3141-3156.	7.9	25
14	A 5.2 GHz RF Energy Harvester System Using Reconfigurable Parallel Rectenna. , 2018, , .		4
15	Design of Peak Efficiency of 85.3% WPC/PMA Wireless Power Receiver Using Synchronous Active Rectifier and Multi Feedback Low-Dropout Regulator. Energies, 2018, 11, 479.	3.1	4
16	Single Inductor-Multiple Output DPWM DC-DC Boost Converter with a High Efficiency and Small Area. Energies, 2018, 11, 725.	3.1	5
17	Modeling of Reference Injection Based Low-Power All-Digital Phase-Locked Loop for Bluetooth Low-Energy Applications in Lab VIEW. , 2018, , .		0
18	An ultra low power fully synthesizable digital phase and frequency detector for ADPLL applications in 55 nm CMOS technology. , 2017, , .		0

#	ARTICLE	IF	CITATIONS
19	Internal circuit offset auto compensation current sensor for wireless power systems. , 2017, , .		0
20	Low power FSK transceiver using ADPLL with direct modulation and integrated SPDT for BLE application. , 2016, , .		4
21	A design of inductive coupling wireless power receiver with high efficiency Active Rectifier and multi feedback LDO regulator. , 2016, , .		1
22	A design of wide input range triple-mode active rectifier with peak efficiency of 94.2% and maximum output power of 8W for wireless power receiver in 0.18μm BCD. Analog Integrated Circuits and Signal Processing, 2016, 86, 255-265.	1.4	5
23	A Design of a Wireless Power Receiving Unit With a High-Efficiency 6.78-MHz Active Rectifier Using Shared DLLs for Magnetic-Resonant A4 WP Applications. IEEE Transactions on Power Electronics, 2016, 31, 4484-4498.	7.9	64
24	A design of 50/150/200kbps, low power FSK transceiver using phase-locked loop with programmable loop bandwidth and integrated SPDT for IEEE 802.15.4g application. Analog Integrated Circuits and Signal Processing, 2015, 84, 261-282.	1.4	1
25	A 1.248~2.918Gb/s low-power transmitter for MIPI M-PHY with 2-step impedance calibration loop in 0.11μm CMOS. Analog Integrated Circuits and Signal Processing, 2015, 83, 129-142.	1.4	2